GigaDevice Semiconductor Inc.

GD30LD2010x
High PSRR Low Dropout LDO

Datasheet

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1 Features

- 1.5V-7.0V input range
- 0.8V~5.0V output range
- ±1.5% output voltage accuracy
- <0.1uA shutdown current
- High PSRR : 80dB@1KHz
- Low Dropout Voltage：520mV@500mA@V_{OUT}=1.8V
- 40uA quiescent current
- Thermal shutdown protection
- Current limit protection
- RoHS Compliant and Halogen Free

2 Applications

- Battery-power equipment
- Portable electric devices
- Audio/Video equipment

3 General description

The GD30LD2010x is a high PSRR low dropout linear regulator with 500mA driving current, which shows good power dissipation with <0.1uA shutdown current and 40uA quiescent current of light load for portable devices. The GD30LD2010x provides 0.8~5.0V output voltage for multiple application and it is with build-in thermal shutdown and current limit protection functions.

4 Device overview

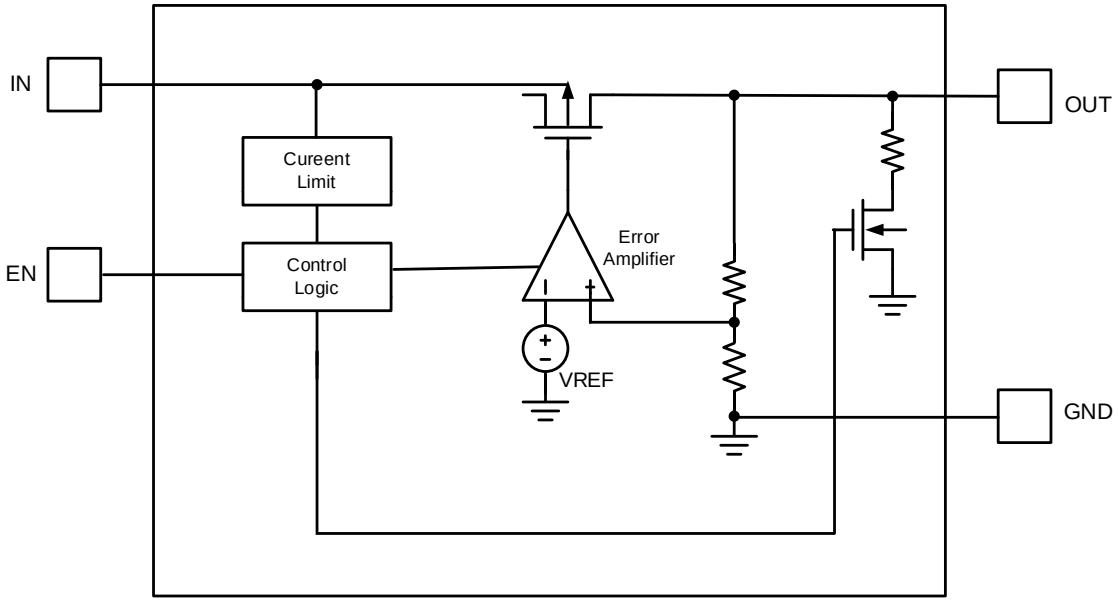
4.1 Device information

Table 4-1 Device information for GD30LD2010x

Part Number	Package	Function	Description
GD30LD2010x	SOT23-5 / DFN	With EN enable pin	500mA high PSRR LDO

4.2 Block diagram

Figure 4-1 Block diagram for GD30LD2010x



4.3 Pinout and pin assignment

Figure 4-2 GD30LD2010x SOT23-5 pinouts

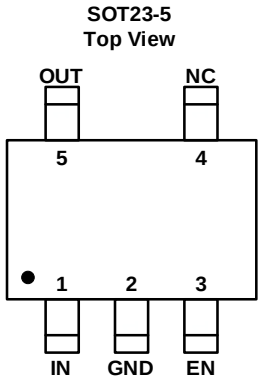
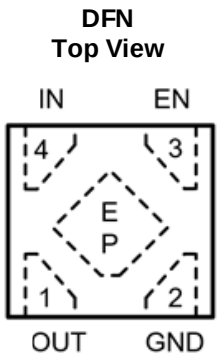


Figure 4-3 GD30LD2010x DFN pinouts



4.4 Pin definitions

Table 4-2 GD30LD2010x SOT23-5 pin definitions

Pin Name	Pins	Pin Type	Functions description
IN	1	P/I	Input of the regulator.
GND	2	G	Ground.
EN	3	I	Enable control input, Active High.
NC	4	-	No Internal Connection.
OUT	5	O	Output of the regulator.
EXPOSED PAD	--	G	The exposed pad should be connected to a large ground plane to maximize thermal performance.

Table 4-3 GD30LD2010x DFN pin definitions

Pin Name	Pins	Pin Type	Functions description
OUT	1	P/I	Output of the regulator.
GND	2	G	Ground.
EN	3	I	Enable control input, Active High.
IN	4	P/I	Input of the regulator.
EXPOSED PAD	--	G	The exposed pad should be connected to a large ground plane to maximize thermal performance.

Notes:

1. Type: I = input, O = output, I/O = input or output, P = power, G = Ground.

5 Functional description

5.1 Recommended device selection

The external input and output capacitors of GD30LD2010x series must be properly selected for stability and performance. Use a 1μF or larger input capacitor and place it close to the IC's IN and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance between 1μF and 22μF requirement may be used. Place the output capacitor close to the IC's OUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

5.2 Dropout voltage

The GD30LD2010x series use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the R_{DS}(ON) of the PMOS pass element. V_{DROP} scales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

5.3 Enable function

The GD30LD2010x series has an EN pin to turn on or turn off the regulator, When the EN pin is in logic high, the regulator will be turned on. When the EN pin is in logic low, the shutdown current is almost 0μA typical. The EN pin may be directly tied to IN to keep the part on.

5.4 Auto discharge function

The GD30LD2010x series can discharge the output capacitor. When the IN ready and EN pin is in logic low, the internal NMOS between OUT and GND will be turned on. The discharge resistance (Rdischg) is 200Ω.

5.5 Current limit

The GD30LD2010x series contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 650mA (typical). The output can be shorted to ground indefinitely without damaging the part.

5.6 OTP(Over Temperature Protection)

The over temperature protection function of GD30LD2010x series will turn off the P-MOSFET when the junction temperature exceeds 165°C (typical). Once the junction temperature cools down by approximately 20°C, the regulator will automatically resume operation.

5.7 Power Dissipation (PD)

Circuit reliability demands that proper consideration is given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

Power dissipation in the regulator depends on the input-to-output voltage difference and load conditions.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

$V_{IN} \times I_{GND}$ represents the static power consumption of the LDO, the value is relatively small and can be ignored. An important note is that power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The main heat conduction path for the device is through the thermal pad on the package. As such, the thermal pad must be soldered to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB, device package, and the temperature of the ambient air (T_A). The maximum power dissipation can be calculated as below:

$$T_J = T_A + \theta_{JA} \times P_D$$

$$I_{OUT} = \left(T_J - T_A\right) / \left[\theta_{JA} \times \left(V_{IN} - V_{OUT}\right)\right]$$

P_D (Max) = (125°C − 25°C) / (250°C/W) = 0.4W

5.8 Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the GD30LD2010x ground pin using as wide and as short of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

6 Electrical characteristics

6.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 6-1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
Voltage	IN, EN, OUT	-0.3	8.0	V
Current	OUT	Internally limited	Internally limited	A
P_D	Power Dissipation @ TA = 25°C	—	0.4	W
Thermal characteristics				
T_J	Operating junction temperature	-55	150	°C
T_{stg}	Storage temperature	-55	150	°C

6.2 Recommended Operating Conditions

Table 6-2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input voltage range	1.5	—	7.0	V
V_{OUT}	Output voltage range	0.8	—	5.0	V
V_{EN}	Enable Voltage range	0	—	V_{IN}	V
I_{OUT}	Output current	0	—	0.5	A
C_{IN}	Input capacitor	1	—	22	uF
C_{OUT}	Output capacitor	1	—	22	uF
T_J	Operating junction temperature	-40	—	125	℃

6.3 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharges (ESD) are applied directly to the pins of the sample.

Table 6-3 Electrostatic Discharge characteristics

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; JS-001-2017	±2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; JS-002-2018	±200	V

6.4 Electrical Specifications

Typical values are at T_A = 25°C. V_{IN} = V_{EN} = 5V, C_{IN} = 1 μF, C_{OUT} = 1 μF, unless otherwise noted.

Table 6-4 Electrical characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Input Range	—		1.5	—	7.0	V
V_{OUT}	Output Voltage Range	-		0.8 -1.5%	—	5.0 +1.5%	V
	Output Accuracy	V_{IN} = V_{OUT} + 1 V, I_{OUT} = 10 mA		-1.5	—	1.5	%
△V_{OUT}/ △V_{IN}	Line Regulation	I_{OUT} = 10 mA, V_{IN} = V_{OUT} + (1 V to 7 V)		—	1	10	mV/V
△V_{OUT}/ △I_{OUT}	Load Regulation	1 mA ≤ I_{OUT}≤ 500 mA		—	2	10	mV/A
V_{DROP} (Note2)	Dropout Voltage	V_{OUT} =1.8V, I_{OUT} = 100mA,		—	520	—	mV
I_{LIM}	Output Current Limit	V_{IN} = 5V, V_{OUT} = 90% * $V_{OUT(TARGET)}$		500	650	—	mA
I_{SC}	Short-Circuit Current Limit	V_{OUT}=0V		—	70	—	mA
I_{SD}	Shut Down Current	EN=0V		—	0.01	0.1	uA
I_{GND}	Quiescent Current	V_{EN} = V_{IN}=6.5V , no load		—	40	60	uA
V_{EN_H}	EN Pin High-Level	—		1.5	—	—	V
V_{EN_L}	EN Pin Low-Level	—		—	—	0.4	V
PSRR	Power Supply Ripple Rejection	I_{OUT} = 50 mA,	f =201 Hz,	—	90	—	dB
		I_{OUT} = 50 mA,	f =1K Hz,	—	80	—	dB
		I_{OUT} = 50 mA,	f =10K Hz,	—	65	—	dB
V_N	Output Noise Voltage	BW = 10 Hz to 100 KHz, C_{OUT} = 1 uF		—	50	—	uV_{RMS}
Rdischg	Output Discharge Resistance	V_{IN}= V_{OUT}+1V,EN=0V		—	200	—	Ω

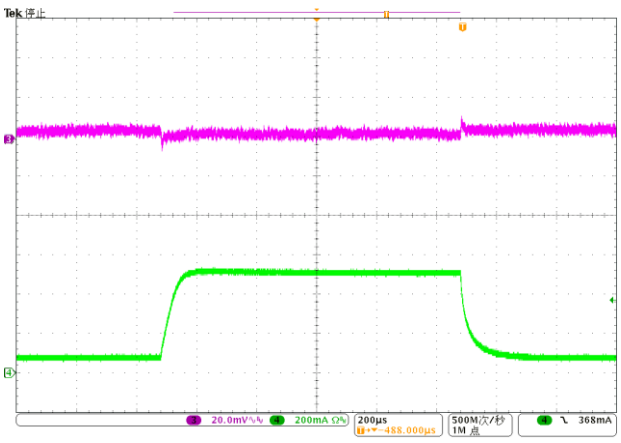
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{SD}	Thermal Shutdown Threshold	Shut down, temperature increasing	—	155	—	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	—	—	20	—	°C

Notes:

1. Stresses beyond those listed “Absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. The dropout voltage is defined as $V_{IN} - V_{OUT}$, when V_{OUT} is 95% of the normal value of V_{OUT}.

6.5 Typical Characteristics

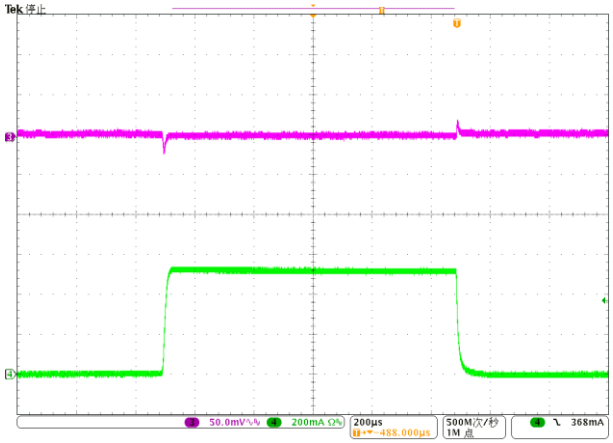
T_A = 25°C, C_{OUT} = 1 uF, C_{IN} = 1 uF (unless otherwise noted).



CH3 = V_{OUT}, CH4 = I_{OUT},

V_{IN} = V_{EN}, V_{OUT} = 1.8V, I_{OUT} = 100mA ~ 500mA

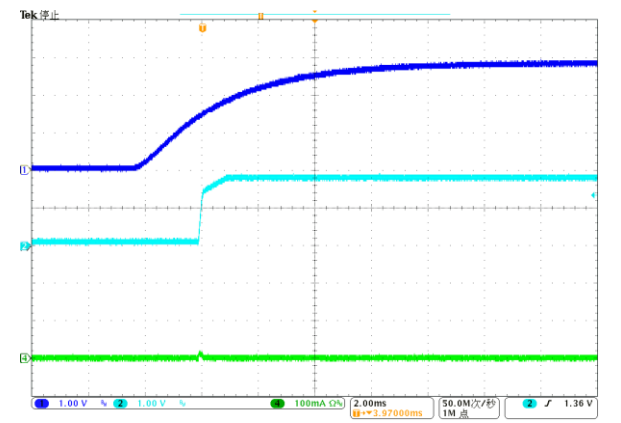
Load Transient



CH3 = V_{OUT}, CH4 = I_{OUT},

V_{IN} = V_{EN}, V_{OUT} = 1.8V, I_{OUT} = 1mA ~ 500mA

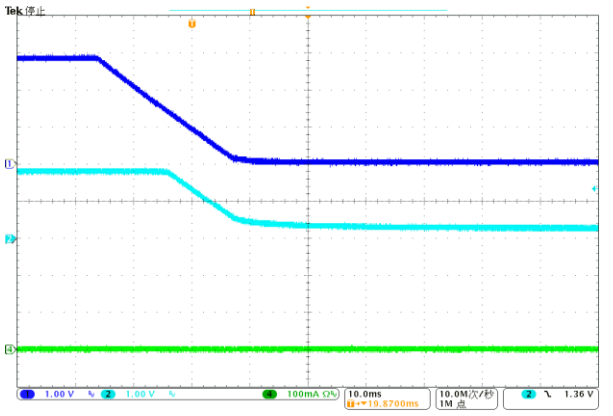
Load Transient



CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

V_{IN} =V_{EN}, V_{OUT} = 1.8V, I_{OUT} = No Load

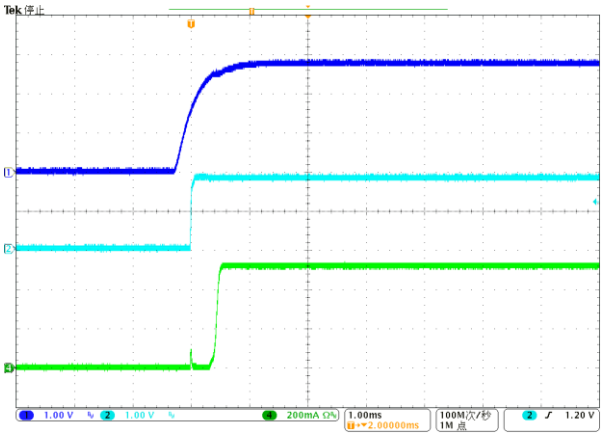
Power On



CH1 = V_{IN}, CH2 = V_{OUT}, CH4 = I_{OUT}

V_{IN} =V_{EN}, V_{OUT} = 1.8V, I_{OUT} = No Load

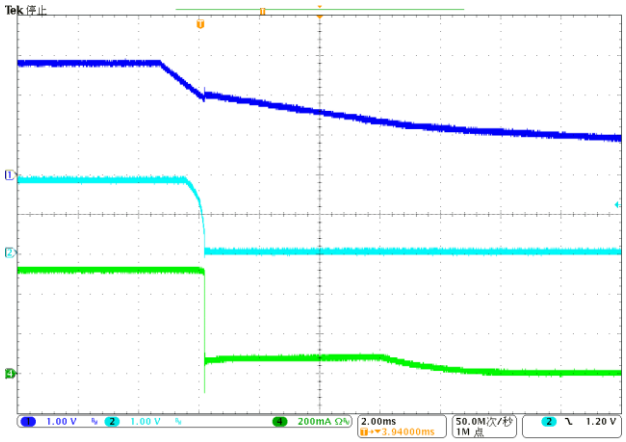
Power Off



$CH1 = V_{IN}$, $CH2 = V_{OUT}$, $CH4 = I_{OUT}$

$V_{IN} = V_{EN}$, $V_{OUT} = 1.8V$, $I_{OUT} = 500mA$

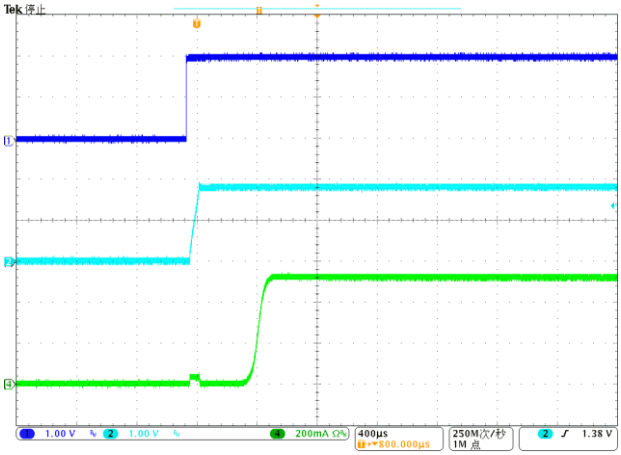
Power On



$CH1 = V_{IN}$, $CH2 = V_{OUT}$, $CH4 = I_{OUT}$

$V_{IN} = V_{EN}$, $V_{OUT} = 1.8V$, $I_{OUT} = 500mA$

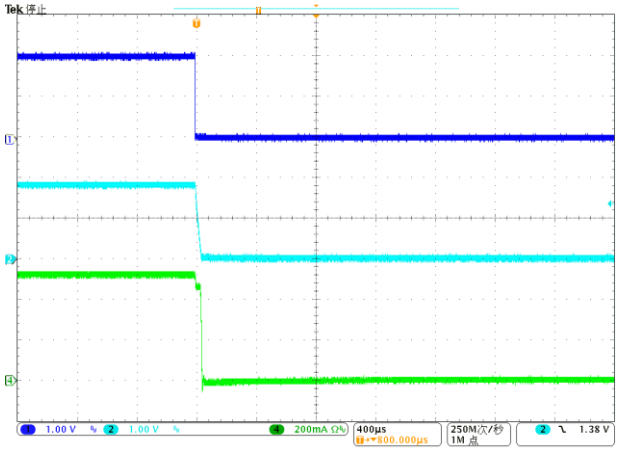
Power Off



$CH1 = V_{EN}$, $CH2 = V_{OUT}$, $CH4 = I_{OUT}$

$V_{IN} = 2.8V$, $V_{OUT} = 1.8V$, $I_{OUT} = 500mA$

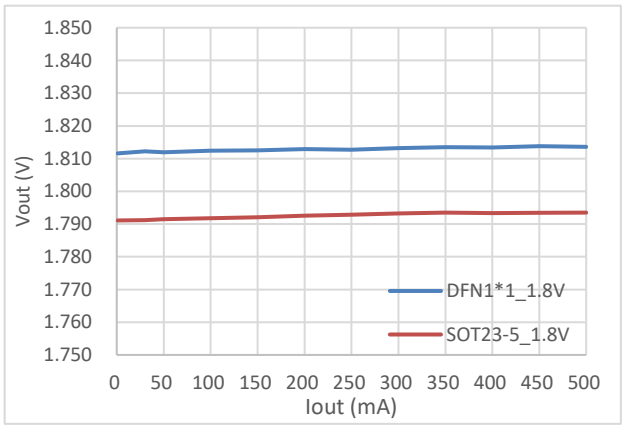
Power On By EN



$CH1 = V_{EN}$, $CH2 = V_{OUT}$, $CH4 = I_{OUT}$

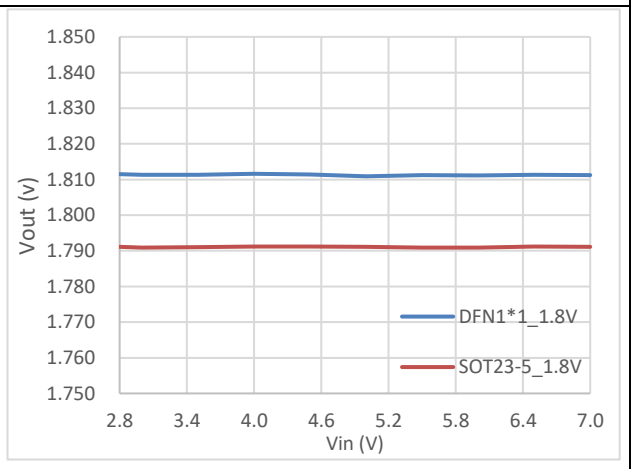
$V_{IN} = 2.8V$, $V_{OUT} = 1.8V$, $I_{OUT} = 500mA$

Power Off By EN



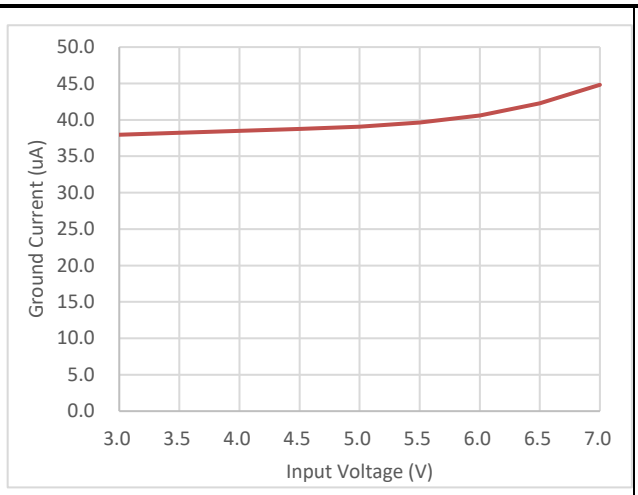
$V_{IN} = 2.8V$, $V_{OUT} = 1.8V$,

Output Voltage VS Output Current



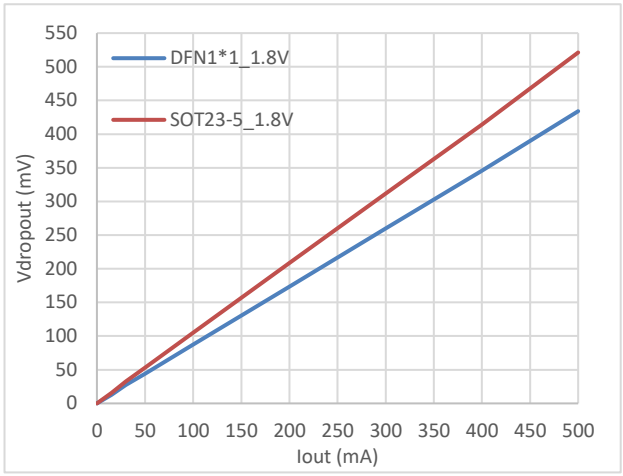
$V_{OUT} = 1.8V$, $I_{OUT} = 1mA$

Output Voltage VS Input Voltage



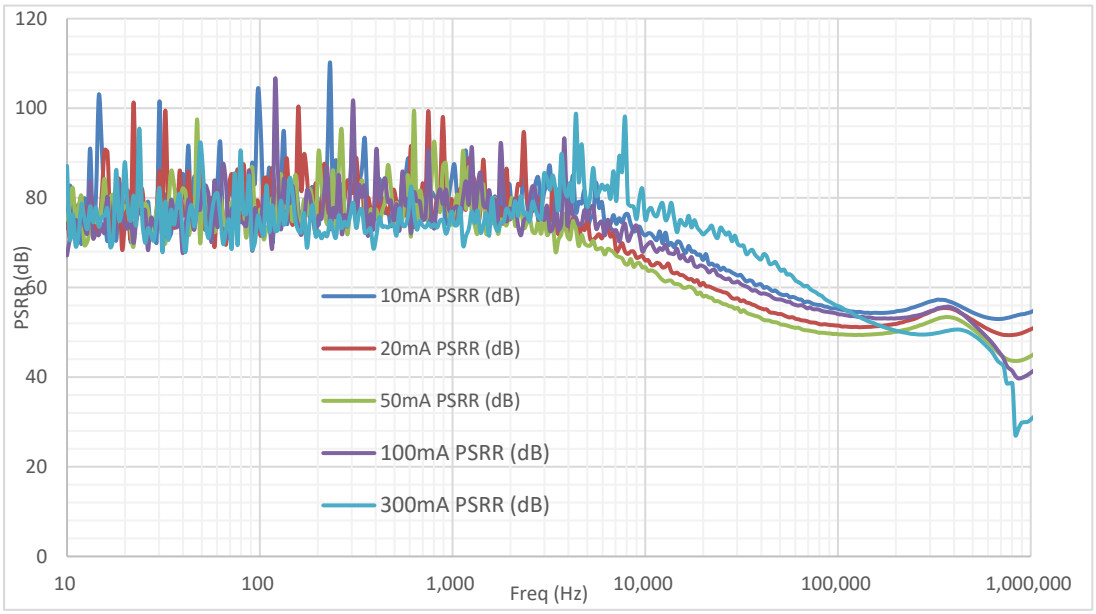
V_{OUT} = 1.8V,No Load

Ground Current VS Input Voltage



V_{OUT} = 1.8V,

Dropout Voltage VS Output Current

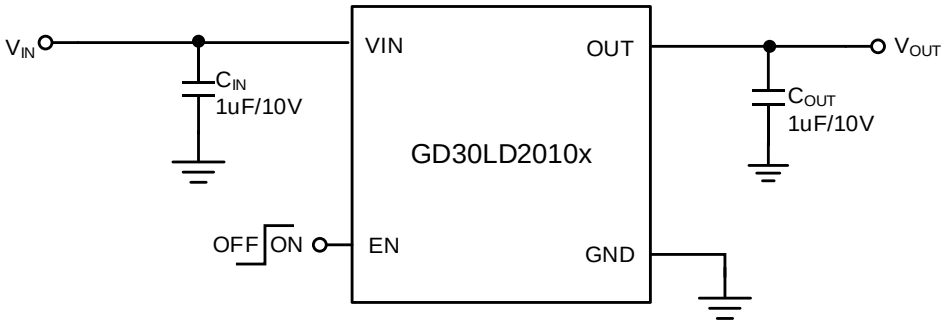


V_{IN} = 2.8V,

PSRR vs Frequency

7 Typical application circuit

Figure 7-1 Typical GD30LD2010x application circuit



8 Package information

8.1 SOT23-5 package outline dimensions

Figure 8-1 SOT23-5 package outline

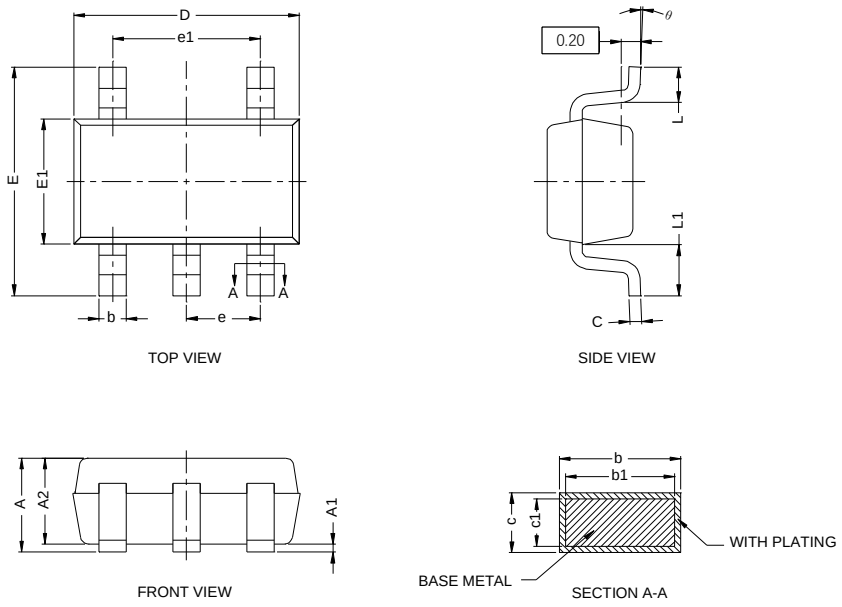


Table 8-1 SOT23-5 dimensions

Symbol	Min	Typ	Max
A	1.05	—	1.25
A1	0.00	—	0.10
A2	1.05	—	1.15
b	0.30	—	0.50
c	0.10	—	0.20
D	2.82	—	3.02
E	2.65	—	2.95
E1	1.50	—	1.70
e	0.95(BSC)		
e1	1.80	—	2.00
L	0.30	0.40	0.60
L1	0.60REF		
θ	0°	—	8°

(Original dimensions are in millimeters)

8.2 DFN package outline dimensions

Figure 8-2 DFN package outline

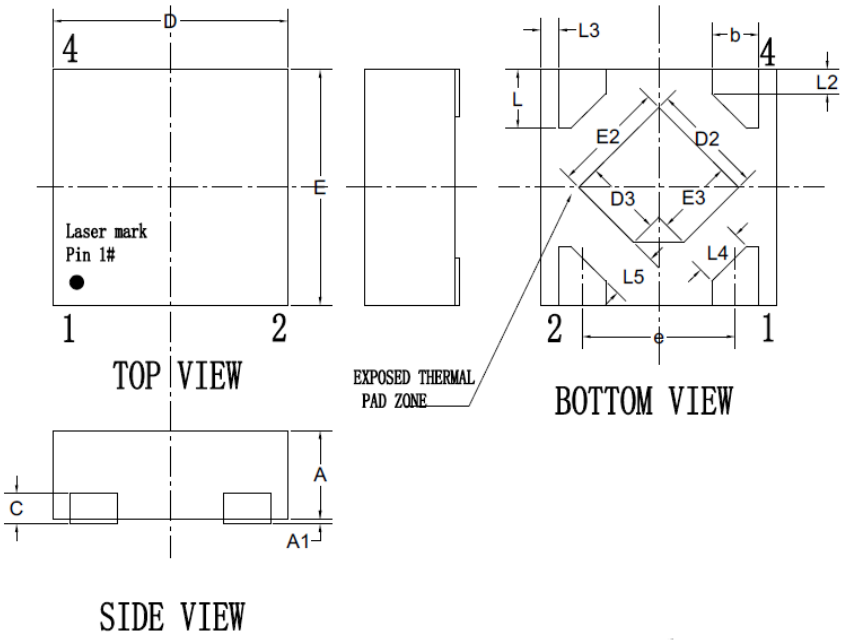


Table 8-2 DFN dimensions

Symbol	Min	Typ	Max
A	0.350	—	0.400
A1	0.000	0.020	0.050
b	0.150	0.200	0.250
C		0.127REF	
D	0.950	1.000	1.050
D2	0.380	0.480	0.580
D3	0.230	0.330	0.430
e		0.650(BSC)	
E	0.950	1.00	1.050
E2	0.38	0.480	0.580
E3	0.230	0.330	0.430
L	0.200	0.250	0.300
L2		0.103REF	
L3		0.075REF	
L4		0.208REF	
L5		0.200REF	

(Original dimensions are in millimeters)

8.3 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "Θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$\Theta_{JA} = (T_J - T_A)/P_D$

$\Theta_{JB} = (T_J - T_B)/P_D$

$\Theta_{JC} = (T_J - T_C)/P_D$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

Θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 8-3 Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
Θ_{JA}	Natural convection, 2S2P PCB	SOT23-5	250.00	°C/W
Θ_{JA}	Natural convection, 2S2P PCB	DFN	250.00	°C/W

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

9 Ordering information

Table 9-1 Part ordering code for GD30LD2010x devices

Ordering Code	V_{OUT}	Package	Package Type	Packing Type	MOQ	Temperature Junction Range
GD30LD2010NSTR-I08	0.8V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I10	1.0V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I12	1.2V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I15	1.5V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I18	1.8V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I25	2.5V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I28	2.8V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I30	3.0V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I33	3.3V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I36	3.6V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010NSTR-I50	5.0V	SOT23-5	Green	Tape&Reel	3000	Industrial -40°C to +125°C
GD30LD2010JETR-I08	0.8V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I10	1.0V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I12	1.2V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I15	1.5V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I18	1.8V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I25	2.5V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I28	2.8V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I30	3.0V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I33	3.3V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I36	3.6V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C
GD30LD2010JETR-I50	5.0V	DFN 1x1	Green	Tape&Reel	10000	Industrial -40°C to +125°C

10 Revision history

Table 10-1 Revision history

Revision No.	Description	Date
0.1	Initial Preliminary Release	May.12, 2023
1.0	V1.0 Release	Jul.20, 2023

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