GigaDevice Semiconductor Inc.

GD32H757xx
Arm® Cortex®-M7 32-bit MCU

Datasheet

Revision 1.3

(Mar. 2024)

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1. General description

The GD32H757xx device belongs to the high performance line of GD32 MCU family. It is a new 32-bit general-purpose microcontroller based on the Arm® Cortex®-M7 core with best cost-performance ratio in terms of enhanced processing capacity, reduced power consumption and peripheral set. The Arm® Cortex®-M7 processor is a highly efficient high-performance, embedded processor that features low interrupt latency, low-cost debug, and has backwards compatibility with existing Cortex-M profile processors. The processor has an in-order super-scalar pipeline that means many instructions can be dual-issued, including load/load and load/store instruction pairs because of multiple memory interfaces. The Cortex-M7 is a high-performance processor, which features a 6-stage superscalar pipeline with branch prediction and an optional FPU capable of single-precision and optionally double-precision operations. The instruction and data buses have been enlarged to 64-bit wide over the previous 32-bit buses. It also provides a Memory Protection Unit (MPU) and powerful trace technology for enhanced application security and advanced debug support.

The GD32H757xx device incorporates the Arm® Cortex®-M7 32-bit processor core operating at 600 MHz frequency with Flash security protection to prevent illegal code/data access. It provides up to 3840 KB on-chip Flash memory, 512KB AXI SRAM and 512KB RAM shared (ITCM/DTCM/AXI) memory. An extensive range of enhanced I/Os and peripherals connected to four APB buses. The devices offer up to two 14-bit 4 MSPS ADCs, a 12 bit 5.3 MSPS ADC, a 12-bit DAC, up to twelve general 16-bit timers, two 16-bit PWM advanced timers, four 32-bit general timers, and four 16-bit basic timers, as well as standard and advanced communication interfaces: up to six SPIs, two OSPIs, four I2Cs, four USARTs and four UARTs, four I2Ss, three CAN-FDs, a USBHS, a ENET, two SDIOs and a MDIO. Additional peripherals as digital camera interface (DCI), EXMC interface with SDRAM extension support, TFT-LCD Interface (TLI), Image Processing Accelerator (IPA), Serial Audio Interface (SAI), Receiver of Sony/Philips Digtial Interface (RSPDIF), Filter arithmetic accelerator (FAC), Real-time decryption (RTDEC) and high performance digital filter module (HPDF) are included.

The device operates from a 1.71V to 3.6V power supply and available in –40 to +85 °C temperature range. Three power saving modes provide the flexibility for maximum optimization of power consumption, an especially important consideration in low power applications.

The above features make GD32H757xx devices suitable for a wide range of interconnection and advanced applications, especially in areas such as industrial control, consumer and handheld equipment, embedded modules, human machine interface, security and alarm systems, energy storage system, graphic display, audio player, automotive navigation, drone, IoT and so on.

2. Device overview

2.1. Device information

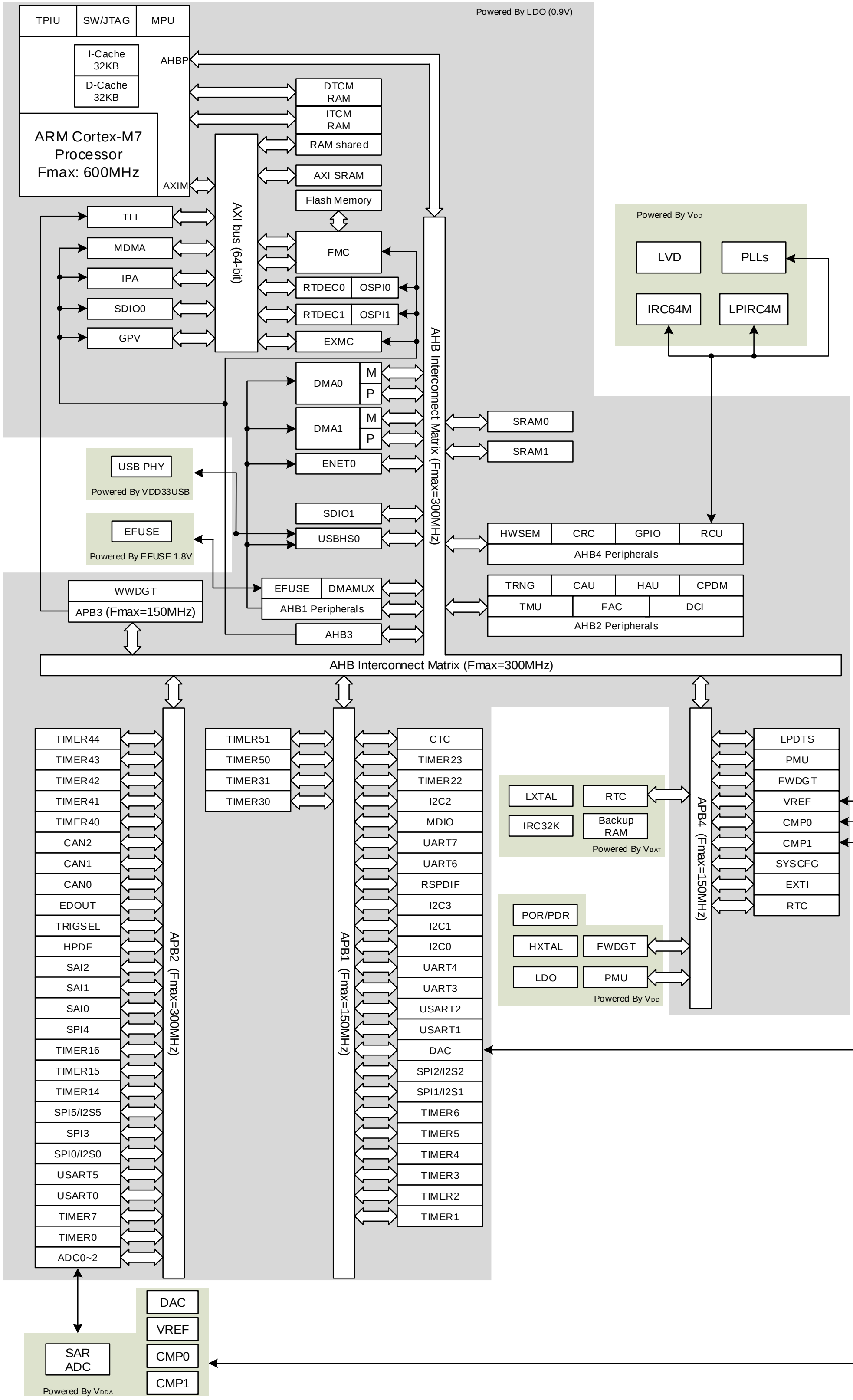
Table 2-1. GD32H757xx devices features and peripheral list

Part Number		GD32H757								
		VGT6	VIT6	VMT6	VGJ6	VIJ6	VMJ6	ZGT6	ZIT6	ZMT6
FLASH (KB)		1024	2048	3840	1024	2048	3840	1024	2048	3840
SRAM (KB)		1024	1024	1024	1024	1024	1024	1024	1024	1024
Timers	General timer (16-bit)	10 (2-3,14-16,40-44)	10 (2-3,14-16,40-44)	10 (2-3,14-16,40-44)	10 (2-3,14-16,40-44)	10 (2-3,14-16,40-44)	10 (2-3,14-16,40-44)	12 (2-3,14-16,30-31,40-44)	12 (2-3,14-16,30-31,40-44)	12 (2-3,14-16,30-31,40-44)
	General timer (32-bit)	4 (1,4,22-23)	4 (1,4,22-23)	4 (1,4,22-23)	4 (1,4,22-23)	4 (1,4,22-23)	4 (1,4,22-23)	4 (1,4,22-23)	4 (1,4,22-23)	4 (1,4,22-23)
	Advanced timer(16-bit)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)	2 (0,7)
	Basic timer (32-bit)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)	2 (5,6)
	Basic timer (64-bit)	2 (50,51)	2 (50,51)	2 (50,51)	2 (50,51)	2 (50,51)	2 (50,51)	2 (50,51)	2 (50,51)	2 (50,51)
	SysTick	1	1	1	1	1	1	1	1	1
	Watchdog	2	2	2	2	2	2	2	2	2
	RTC	1	1	1	1	1	1	1	1	1
Connectivity	USART	4	4	4	4	4	4	4	4	4
	UART	4	4	4	4	4	4	4	4	4
	I2C	4	4	4	4	4	4	4	4	4
	SPI/I2S	5/4 (0-3,5)/(0-2,5)	5/4 (0-3,5)/(0-2,5)	5/4 (0-3,5)/(0-2,5)	5/4 (0-3,5)/(0-2,5)	5/4 (0-3,5)/(0-2,5)	5/4 (0-3,5)/(0-2,5)	6/4 (0-5)/(0-2,5)	6/4 (0-5)/(0-2,5)	6/4 (0-5)/(0-2,5)
	OSPI	1	1	1	1	1	1	2	2	2
	SDIO	2	2	2	2	2	2	2	2	2
	MDIO	1	1	1	1	1	1	1	1	1
	CAN	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD	3xFD
	USBHS	1	1	1	1	1	1	1	1	1
	ENET	1	1	1	1	1	1	1	1	1
	TLI	1	1	1	1	1	1	1	1	1

Part Number		GD32H757								
		VGT6	VIT6	VMT6	VGJ6	VIJ6	VMJ6	ZGT6	ZIT6	ZMT6
	DCI	1	1	1	1	1	1	1	1	1
SAI		2	2	2	2	2	2	3	3	3
RSPDIF		1	1	1	1	1	1	1	1	1
HPDF		1	1	1	1	1	1	1	1	1
EXMC/SDRAM		1/0	1/0	1/0	1/0	1/0	1/0	1/1	1/1	1/1
IPA		1	1	1	1	1	1	1	1	1
FAC		1	1	1	1	1	1	1	1	1
EDOUT		1	1	1	1	1	1	1	1	1
CPDM		2	2	2	2	2	2	2	2	2
RTDEC		2	2	2	2	2	2	2	2	2
TMU		1	1	1	1	1	1	1	1	1
14bit ADC	Units	2	2	2	2	2	2	2	2	2
	Channels	14,12	14,12	14,12	14,12	14,12	14,12	16,14	16,14	16,14
12bit ADC	Units	1	1	1	1	1	1	1	1	1
	Channels	4	4	4	4	4	4	12	12	12
DAC	Units	1	1	1	1	1	1	1	1	1
	Channels	2	2	2	2	2	2	2	2	2
CMP		2	2	2	2	2	2	2	2	2
GPIO		82	82	82	82	82	82	113	113	113
Package		LQFP100			BGA100			LQFP144		

2.2. Block diagram

Figure 2-1. GD32H757xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32H757Vx BGA100 pinouts

	1	2	3	4	5	6	7	8	9	10
A	PC14	PC13	PE2	PB9	PB7	PB4	PB3	PA15	PA14	PA13
B	PC15	VBAT	PE3	PB8	PB6	PD5	PD2	PC11	PC10	USBH S0_DP
C	PH0	VSS	PE4	PE1	PB5	PD6	PD3	PC12	PA9	USBH S0_DM
D	PH1	VDD	PE5	PE0	BOOT	PD7	PD4	PD0	PA8	PA10
E	NRST	PC2_C	PE6	VSS	VSS	VSS	VCORE	PD1	PC9	PC7
F	PC0	PC1	PC3_C	VDD	VDD	VDD33 USB	PDR_ON	VCORE	PC8	PC6
G	VSSA	PA0	PA4	PC4	PB2	PE10	PE14	PD15	PD11	PB15
H	VDDA	PA1	PA5	PC5	PE7	PE11	PE15	PD14	PD10	PB14
J	VSS	PA2	PA6	PB0	PE8	PE12	PB10	PB13	PD9	PD13
K	VDD	PA3	PA7	PB1	PE9	PE13	PB11	PB12	PD8	PD12

GigaDevice GD32H757Vx
BGA100

Figure 2-3. GD32H757Zx LQFP144 pinouts

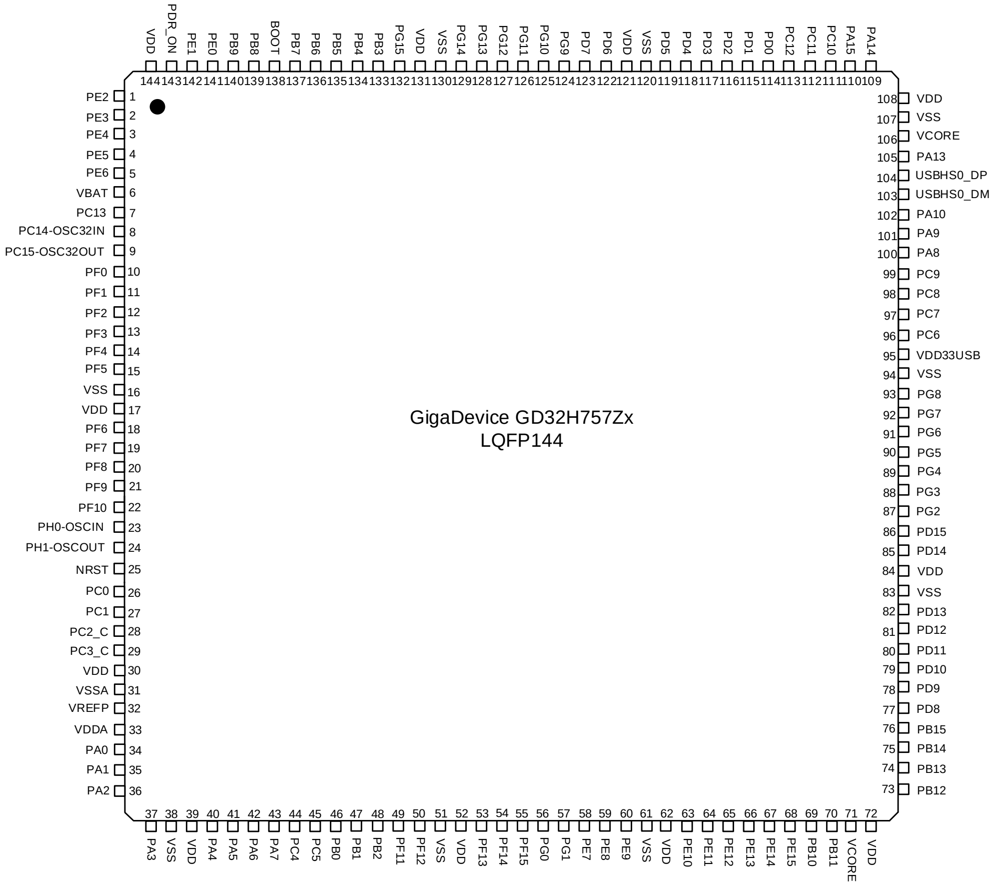
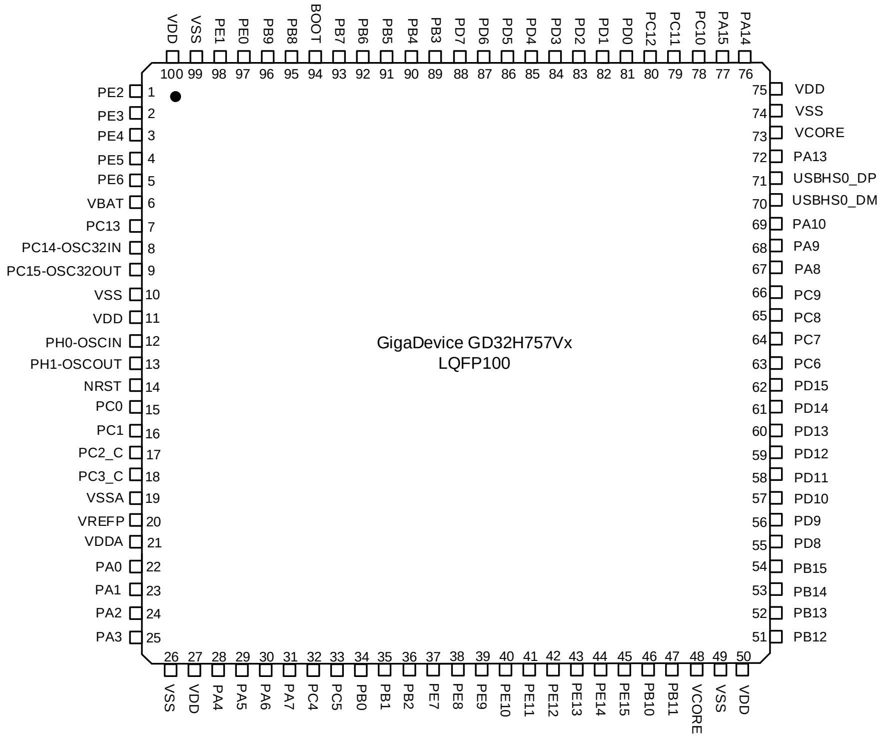


Figure 2-4. GD32H757Vx LQFP100 pinouts



2.4. Memory map

Table 2-2. GD32H757xx memory map

Pre-defined Regions	Bus	Address	Peripherals
External RAM		0xD000 0000 - 0xDFFF FFFF	EXMC - SDRAM device 1
		0xC000 0000 - 0xCFFF FFFF	EXMC - SDRAM device 0 (EXMC Bank 0 Region 0-3)
		0xA000 1000 - 0xBFFF FFFF	Reserved
		0xA000 0000 - 0xA000 0FFF	Reserved
		0x9000 0000 - 0x9FFF FFFF	OSPI0
		0x8000 0000 - 0x8FFF FFFF	EXMC - NAND
		0x7000 0000 - 0x7FFF FFFF	OSPI1
		0x6000 0000 - 0x6FFF FFFF	EXMC - NOR/PSRAM/SRAM
Peripheral	AHB4	0x5802 7000 - 0x5FFF FFFF	Reserved
		0x5802 6400 - 0x5802 67FF	HWSEM
		0x5802 6000 - 0x5802 63FF	Reserved
		0x5802 5000 - 0x5802 5FFF	Reserved
		0x5802 4C00 - 0x5802 4FFF	CRC
		0x5802 4800 - 0x5802 4BFF	Reserved
		0x5802 4400 - 0x5802 47FF	RCU

Pre-defined Regions	Bus	Address	Peripherals
		0x5802 2C00 - 0x5802 43FF	Reserved
		0x5802 2800 - 0x5802 2BFF	GPIOK
		0x5802 2400 - 0x5802 27FF	GPIOJ
		0x5802 2000 - 0x5802 23FF	Reserved
		0x5802 1C00 - 0x5802 1FFF	GPIOH
		0x5802 1800 - 0x5802 1BFF	GPIOG
		0x5802 1400 - 0x5802 17FF	GPIOF
		0x5802 1000 - 0x5802 13FF	GPIOE
		0x5802 0C00 - 0x5802 0FFF	GPIOD
		0x5802 0800 - 0x5802 0BFF	GPIOC
		0x5802 0400 - 0x5802 07FF	GPIOB
		0x5802 0000 - 0x5802 03FF	GPIOA
		0x5801 0000 - 0x5801 FFFF	Reserved
	APB4	0x5800 7400 - 0x5800 FFFF	Reserved
		0x5800 7000 - 0x5800 73FF	Reserved
		0x5800 6C00 - 0x5800 6FFF	Reserved
		0x5800 6800 - 0x5800 6BFF	LPDTS
		0x5800 5800 - 0x5800 67FF	PMU
		0x5800 5400 - 0x5800 57FF	Reserved
		0x5800 4C00 - 0x5800 53FF	Reserved
		0x5800 4800 - 0x5800 4BFF	FWDGT
		0x5800 4000 - 0x5800 43FF	RTC
		0x5800 3C00 - 0x5800 3FFF	VREF
		0x5800 3800 - 0x5800 3BFF	CMP0 - CMP1
		0x5800 3400 - 0x5800 37FF	Reserved
		0x5800 3000 - 0x5800 33FF	Reserved
		0x5800 2C00 - 0x5800 2FFF	Reserved
		0x5800 2800 - 0x5800 2BFF	Reserved
		0x5800 2400 - 0x5800 27FF	Reserved
		0x5800 2000 - 0x5800 23FF	Reserved
		0x5800 1C00 - 0x5800 1FFF	Reserved
		0x5800 1400 - 0x5800 17FF	Reserved
		0x5800 0800 - 0x5800 13FF	Reserved
		0x5800 0400 - 0x5800 07FF	SYSCFG
		0x5800 0000 - 0x5800 03FF	EXTI
	AHB3	0x5200 C000 - 0x57FF FFFF	Reserved
		0x5200 BC00 - 0x5200 BFFF	RTDEC1
		0x5200 B800 - 0x5200 BBFF	RTDEC0
		0x5200 B400 - 0x5200 B7FF	OSPIM
		0x5200 B000 - 0x5200 B3FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x5200 A000 - 0x5200 AFFF	OSPI1
		0x5200 9400 - 0x5200 9FFF	Reserved
		0x5200 9000 - 0x5200 93FF	RAMECCMU Region 0
		0x5200 8000 - 0x5200 8FFF	CPDM(SDIO0)
		0x5200 7000 - 0x5200 7FFF	SDIO0
		0x5200 6000 - 0x5200 6FFF	Reserved
		0x5200 5000 - 0x5200 5FFF	OSPI0
		0x5200 4000 - 0x5200 4FFF	EXMC
		0x5200 3400 - 0x5200 3FFF	Reserved
		0x5200 3000 - 0x5200 33FF	Reserved
		0x5200 2000 - 0x5200 2FFF	Flash memory interface
		0x5200 1000 - 0x5200 1FFF	IPA
		0x5200 0000 - 0x5200 0FFF	MDMA
		0x5110 0000 - 0x51FF FFFF	Reserved
		0x5100 0000 - 0x510F FFFF	AXI interconnect matrix
	APB3	0x5006 1000 - 0x50FF FFFF	Reserved
		0x5006 0C00 - 0x5006 0FFF	Reserved
		0x5006 0800 - 0x5006 0BFF	Reserved
		0x5006 0400 - 0x5006 07FF	Reserved
		0x5006 0000 - 0x5006 03FF	Reserved
		0x5005 0400 - 0x5005 FFFF	Reserved
		0x5005 0000 - 0x5005 03FF	Reserved
		0x5004 0000 - 0x5004 FFFF	Reserved
		0x5000 0000 - 0x5003 FFFF	Reserved
		0x5000 3000 - 0x5000 3FFF	WWDGT
		0x5000 2000 - 0x5000 2FFF	Reserved
		0x5000 1000 - 0x5000 1FFF	TLI
		0x5000 0000 - 0x5000 0FFF	Reserved
	AHB2	0x4802 5000 - 0x4FFF FFFF	Reserved(AHB2)
		0x4802 4800 - 0x4802 4FFF	FAC
		0x4802 4400 - 0x4802 47FF	TMU
		0x4802 4000 - 0x4802 43FF	Reserved
		0x4802 3000 - 0x4802 3FFF	RAMECCMU Region 1
		0x4802 2C00 - 0x4802 2FFF	Reserved(AHB2)
		0x4802 2800 - 0x4802 2BFF	CPDM(SDIO1)
		0x4802 2400 - 0x4802 27FF	SDIO1
		0x4802 1C00 - 0x4802 23FF	Reserved(AHB2)
		0x4802 1800 - 0x4802 1BFF	TRNG
		0x4802 1400 - 0x4802 17FF	HAU
		0x4802 1000 - 0x4802 13FF	CAU

Pre-defined Regions	Bus	Address	Peripherals
		0x4802 0400 - 0x4802 0FFF	Reserved(AHB2)
		0x4802 0000 - 0x4802 03FF	DCI
		0x4800 1800 - 0x4801 FFFF	Reserved(AHB2)
		0x4800 1400 - 0x4800 17FF	Reserved
		0x4800 1000 - 0x4800 13FF	Reserved
		0x4800 0C00 - 0x4800 0FFF	Reserved
		0x4800 0800 - 0x4800 0BFF	Reserved
		0x4800 0400 - 0x4800 07FF	Reserved
		0x4800 0000 - 0x4800 03FF	Reserved
	AHB1	0x400C 0000 - 0x47FF FFFF	Reserved(AHB1)
		0x4008 0000 - 0x400B FFFF	Reserved
		0x4004 0000 - 0x4007 FFFF	USBHS0
		0x4003 8C00 - 0x4003 FFFF	Reserved
		0x4003 8400 - 0x4003 8BFF	Reserved
		0x4003 8000 - 0x4003 83FF	Reserved
		0x4003 3000 - 0x4003 7FFF	Reserved
		0x4003 0000 - 0x4003 2FFF	Reserved
		0x4002 C000 - 0x4002 FFFF	Reserved
		0x4002 BC00 - 0x4002 BFFF	Reserved
		0x4002 B000 - 0x4002 BBFF	Reserved
		0x4002 A000 - 0x4002 AFFF	Reserved
		0x4002 8000 - 0x4002 9FFF	ENET0
		0x4002 6800 - 0x4002 7FFF	Reserved
		0x4002 6400 - 0x4002 67FF	Reserved
		0x4002 6000 - 0x4002 63FF	Reserved
		0x4002 5000 - 0x4002 5FFF	Reserved
		0x4002 4000 - 0x4002 4FFF	Reserved
		0x4002 3C00 - 0x4002 3FFF	Reserved
		0x4002 3800 - 0x4002 3BFF	Reserved
		0x4002 3400 - 0x4002 37FF	Reserved
		0x4002 3000 - 0x4002 33FF	Reserved
		0x4002 2C00 - 0x4002 2FFF	Reserved
		0x4002 2800 - 0x4002 2BFF	EFUSE
		0x4002 2400 - 0x4002 27FF	Reserved
		0x4002 2000 - 0x4002 23FF	Reserved
		0x4002 1C00 - 0x4002 1FFF	Reserved
		0x4002 1800 - 0x4002 1BFF	Reserved
		0x4002 1400 - 0x4002 17FF	Reserved
		0x4002 1000 - 0x4002 13FF	Reserved
		0x4002 0C00 - 0x4002 0FFF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4002 0800 - 0x4002 0BFF	DMAMUX
		0x4002 0400 - 0x4002 07FF	DMA1
		0x4002 0000 - 0x4002 03FF	DMA0
	APB2	0x4001 F400 - 0x4001 FFFF	Reserved
		0x4001 F000 - 0x4001 F3FF	TIMER44
		0x4001 DC00 - 0x4001 DFFF	TIMER43
		0x4001 D800 - 0x4001 DBFF	TIMER42
		0x4001 D400 - 0x4001 D7FF	TIMER41
		0x4001 D000 - 0x4001 D3FF	TIMER40
		0x4001 C000 - 0x4001 CFFF	CAN2(4KB)
		0x4001 B000 - 0x4001 BFFF	CAN1(4KB)
		0x4001 A000 - 0x4001 AFFF	CAN0(4KB)
		0x4001 8C00 - 0x4001 9FFF	Reserved
		0x4001 8800 - 0x4001 8BFF	EDOUT
		0x4001 8400 - 0x4001 87FF	TRIGSEL
		0x4001 8000 - 0x4001 83FF	Reserved(APB2)
		0x4001 7C00 - 0x4001 7FFF	Reserved
		0x4001 7800 - 0x4001 7BFF	Reserved
		0x4001 7400 - 0x4001 77FF	Reserved
		0x4001 7000 - 0x4001 73FF	HPDF
		0x4001 6C00 - 0x4001 6FFF	Reserved
		0x4001 6800 - 0x4001 6BFF	Reserved
		0x4001 6400 - 0x4001 67FF	Reserved
		0x4001 6000 - 0x4001 63FF	SAI2
		0x4001 5C00 - 0x4001 5FFF	SAI1
		0x4001 5800 - 0x4001 5BFF	SAI0
		0x4001 5400 - 0x4001 57FF	Reserved
		0x4001 5000 - 0x4001 53FF	SPI4
		0x4001 4C00 - 0x4001 4FFF	Reserved
		0x4001 4800 - 0x4001 4BFF	TIMER16
		0x4001 4400 - 0x4001 47FF	TIMER15
		0x4001 4000 - 0x4001 43FF	TIMER14
		0x4001 3C00 - 0x4001 3FFF	Reserved
		0x4001 3800 - 0x4001 3BFF	SPI5/I2S5
		0x4001 3400 - 0x4001 37FF	SPI3
		0x4001 3000 - 0x4001 33FF	SPI0/I2S0
		0x4001 2C00 - 0x4001 2FFF	ADC2
		0x4001 2800 - 0x4001 2BFF	ADC1
		0x4001 2400 - 0x4001 27FF	ADC0
		0x4001 2000 - 0x4001 23FF	Reserved

Pre-defined Regions	Bus	Address	Peripherals
		0x4001 1C00 - 0x4001 1FFF	Reserved
		0x4001 1800 - 0x4001 1BFF	Reserved
		0x4001 1400 - 0x4001 17FF	USART5
		0x4001 1000 - 0x4001 13FF	USART0
		0x4001 0C00 - 0x4001 0FFF	Reserved
		0x4001 0800 - 0x4001 0BFF	Reserved
		0x4001 0400 - 0x4001 07FF	TIMER7
		0x4001 0000 - 0x4001 03FF	TIMER0
	APB1	0x4000 F800 - 0x4000 FFFF	Reserved
		0x4000 F400 - 0x4000 F7FF	TIMER51
		0x4000 F000 - 0x4000 F3FF	TIMER50
		0x4000 EC00 - 0x4000 EFFF	TIMER31
		0x4000 E800 - 0x4000 EBFF	TIMER30
		0x4000 E400 - 0x4000 E7FF	TIMER23
		0x4000 E000 - 0x4000 E3FF	TIMER22
		0x4000 DC00 - 0x4000 DFFF	Reserved
		0x4000 D800 - 0x4000 DBFF	Reserved
		0x4000 D400 - 0x4000 D7FF	Reserved
		0x4000 D000 - 0x4000 D3FF	Reserved
		0x4000 CC00 - 0x4000 CFFF	Reserved
		0x4000 C800 - 0x4000 CBFF	Reserved
		0x4000 C400 - 0x4000 C7FF	Reserved
		0x4000 C000 - 0x4000 C3FF	I2C2
		0x4000 9800 - 0x4000 BFFF	Reserved
		0x4000 9400 - 0x4000 97FF	MDIO
		0x4000 8800 - 0x4000 93FF	Reserved
		0x4000 8400 - 0x4000 87FF	CTC
		0x4000 8000 - 0x4000 83FF	Reserved
		0x4000 7C00 - 0x4000 7FFF	UART7
		0x4000 7800 - 0x4000 7BFF	UART6
		0x4000 7400 - 0x4000 77FF	DAC0/DAC1
		0x4000 7000 - 0x4000 73FF	Reserved
		0x4000 6C00 - 0x4000 6FFF	Reserved
		0x4000 6800 - 0x4000 6BFF	Reserved
		0x4000 6400 - 0x4000 67FF	Reserved
		0x4000 6000 - 0x4000 63FF	Reserved
		0x4000 5C00 - 0x4000 5FFF	I2C3
		0x4000 5800 - 0x4000 5BFF	I2C1
		0x4000 5400 - 0x4000 57FF	I2C0
		0x4000 5000 - 0x4000 53FF	UART4

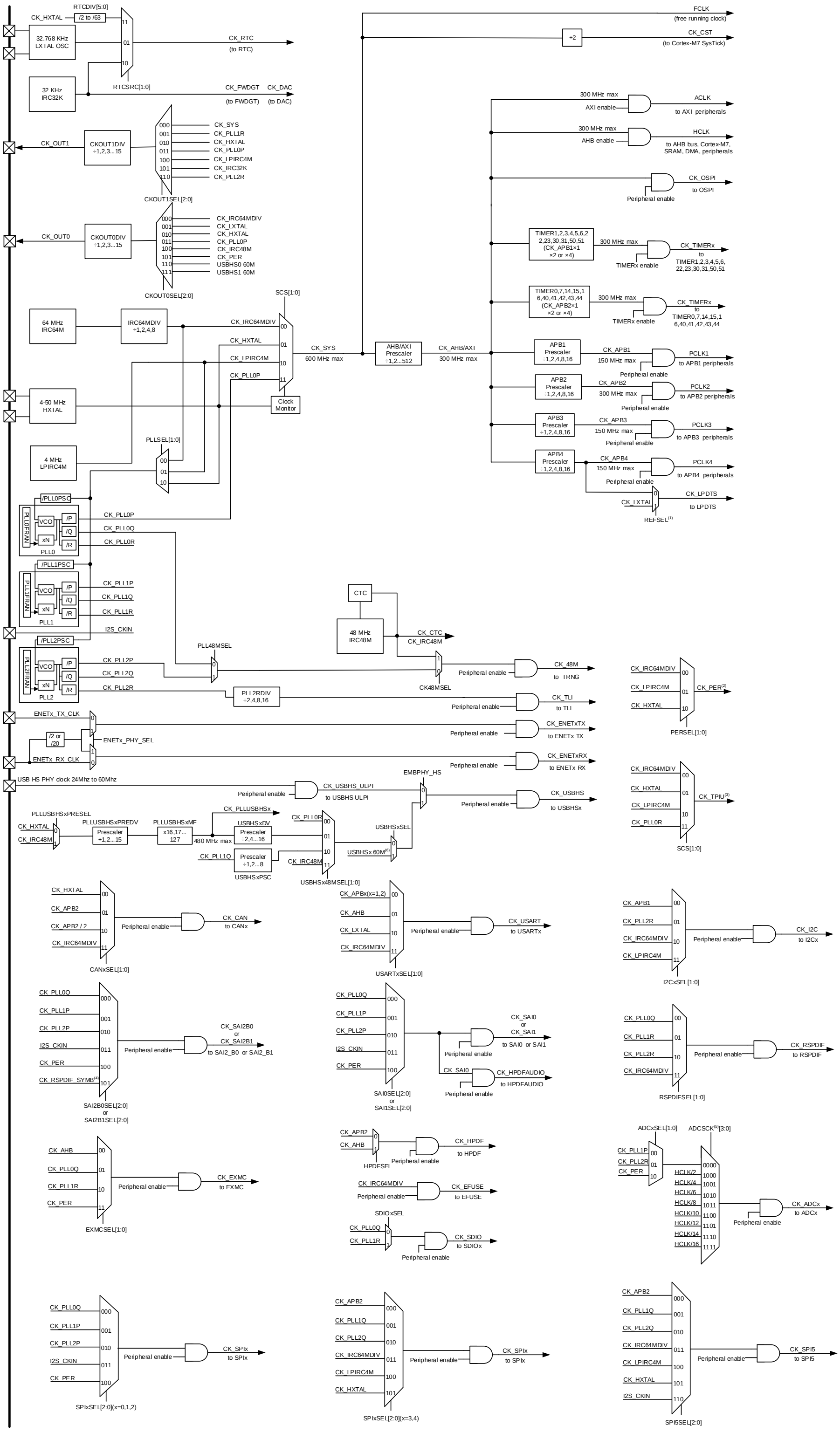
Pre-defined Regions	Bus	Address	Peripherals
		0x4000 4C00 - 0x4000 4FFF	UART3
		0x4000 4800 - 0x4000 4BFF	USART2
		0x4000 4400 - 0x4000 47FF	USART1
		0x4000 4000 - 0x4000 43FF	RSPDIF
		0x4000 3C00 - 0x4000 3FFF	SPI2/I2S2
		0x4000 3800 - 0x4000 3BFF	SPI1/I2S1
		0x4000 3400 - 0x4000 37FF	Reserved
		0x4000 3000 - 0x4000 33FF	Reserved
		0x4000 2C00 - 0x4000 2FFF	Reserved
		0x4000 2800 - 0x4000 2BFF	Reserved
		0x4000 2400 - 0x4000 27FF	Reserved
		0x4000 2000 - 0x4000 23FF	Reserved
		0x4000 1C00 - 0x4000 1FFF	Reserved
		0x4000 1800 - 0x4000 1BFF	Reserved
		0x4000 1400 - 0x4000 17FF	TIMER6
		0x4000 1000 - 0x4000 13FF	TIMER5
		0x4000 0C00 - 0x4000 0FFF	TIMER4
		0x4000 0800 - 0x4000 0BFF	TIMER3
		0x4000 0400 - 0x4000 07FF	TIMER2
		0x4000 0000 - 0x4000 03FF	TIMER1
SRAM		0x3880 1000 - 0x3FFF FFFF	Reserved
		0x3880 0000 - 0x3880 0FFF	Backup SRAM
		0x3000 8000 - 0x387F FFFF	Reserved
		0x3000 4000 - 0x3000 7FFF	SRAM1(16KB)
		0x3000 0000 - 0x3000 3FFF	SRAM0(16KB)
		0x2410 0000 - 0x2FFF FFFF	Reserved
		0x2408 0000 - 0x240F FFFF	RAM(512KB) shared (ITCM/DTCM/AXI)
		0x2400 0000 - 0x2407 FFFF	AXI SRAM(512KB)
		0x2008 0000 - 0x23FF FFFF	Reserved
		0x2007 0000 - 0x2007 FFFF	DTCM RAM(from RAM shared)
		0x2006 0000 - 0x2006 FFFF	
		0x2003 0000 - 0x2005 FFFF	
		0x2002 0000 - 0x2002 FFFF	
		0x2001 C000 - 0x2001 FFFF	
		0x2001 8000 - 0x2001 BFFF	
		0x2001 0000 - 0x2001 7FFF	
		0x2000 D000 - 0x2000 FFFF	
		0x2000 C000 - 0x2000 CFFF	
		0x2000 8000 - 0x2000 BFFF	

Pre-defined Regions	Bus	Address	Peripherals
		0x2000 5000 - 0x2000 7FFF	
		0x2000 2000 - 0x2000 4FFF	
		0x2000 1000 - 0x2000 1FFF	
		0x2000 0000 - 0x2000 0FFF	
Code		0x1FFF FC10 - 0x1FFF FFFF	Reserved
		0x1FFF FC00 - 0x1FFF FC0F	Reserved
		0x1FFF F818 - 0x1FFF BFFF	Reserved
		0x1FFF F800 - 0x1FFF F817	Reserved
		0x1FFF F000 - 0x1FFF F7FF	Reserved
		0x1FFF EC00 - 0x1FFF EFFF	Reserved
		0x1FFF C010 - 0x1FFF EBFF	Reserved
		0x1FFF C000 - 0x1FFF C00F	Reserved
		0x1FFF B000 - 0x1FFF BFFF	Reserved
		0x1FFF 8000 - 0x1FFF AFFF	Reserved
		0x1FFF 7A10 - 0x1FFF 7FFF	Reserved
		0x1FFF 7800 - 0x1FFF 7A0F	Reserved
		0x1FFF 7400 - 0x1FFF 77FF	Reserved
		0x1FFF 7000 - 0x1FFF 73FF	Reserved
		0x1FFF 0000 - 0x1FFF 6FFF	Reserved
		0x1FFE C010 - 0x1FFE FFFF	Reserved
		0x1FFE C000 - 0x1FFE C00F	Reserved
		0x1FF6 0000 - 0x1FFE BFFF	Reserved
		0x1FF4 0000 - 0x1FF5 FFFF	Reserved
		0x1FFF 9000 - 0x1FF3 FFFF	Reserved
		0x1FF0 0000 - 0x1FFF 8FFF	System Memory
		0x1002 0000 - 0x1FEF FFFF	Reserved
		0x1001 0000 - 0x1001 FFFF	Reserved
		0x1000 0000 - 0x1000 FFFF	Reserved
		0x0A00 D000 - 0x0FFF FFFF	Reserved
		0x0A00 C000 - 0x0A00 CFFF	Reserved
		0x0A00 8000 - 0x0A00 BFFF	Reserved
		0x0A00 0000 - 0x0A00 7FFF	Reserved
		0x08C0 1000 - 0x09FF FFFF	Reserved
		0x08C0 0000 - 0x08C0 0FFF	Reserved
		0x0881 0000 - 0x08BF FFFF	Reserved
		0x0880 0000 - 0x0880 FFFF	Reserved
		0x0840 0000 - 0x087F FFFF	Reserved
		0x083C 0000 - 0x083F FFFF	Reserved
		0x0830 0000 - 0x083B FFFF	Flash memory
		0x0810 0000 - 0x082F FFFF	

Pre-defined Regions	Bus	Address	Peripherals
		0x0808 0000 - 0x080F FFFF	
		0x0806 0000 - 0x0807 FFFF	
		0x0802 0000 - 0x0805 FFFF	
		0x0801 0000 - 0x0801 FFFF	
		0x0800 0000 - 0x0800 FFFF	
		0x0030 0000 - 0x07FF FFFF	Reserved
		0x0010 0000 - 0x002F FFFF	Reserved
		0x0008 0000 - 0x000F FFFF	Reserved
		0x0002 6000 - 0x0007 FFFF	ITCM RAM(from RAM shared)
		0x0002 0000 - 0x0002 5FFF	
		0x0001 0000 - 0x0001 FFFF	
		0x0000 0000 - 0x0000 FFFF	

2.5. Clock tree

Figure 2-5. GD32H757xx clock tree



Legend:

HXTAL: High speed crystal oscillator

LXTAL: Low speed crystal oscillator

IRC32K: Internal 32K RC oscillator

IRC48M: Internal 48M RC oscillators

IRC64M: Internal 64M RC oscillators

2.6. Pin definitions

2.6.1. GD32H757Zx LQFP144 pin definitions

Table 2-3. GD32H757Zx LQFP144 pin definitions

LQFP144				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O		Default: PE2 Alternate: TRACECK, SAI0_CLK0, SPI3_SCK, SAI0_MCLK0, SAI2_MCLK0, OSPIM_P0_IO2, SAI2_CLK0, EXMC_A23, EVENTOUT
PE3	2	I/O		Default: PE3 Alternate: TRACED0, TIMER14_BRKIN0, SAI0_SD1, SAI2_SD1, EXMC_A19, DCI_PIXCLK, EVENTOUT
PE4	3	I/O		Default: PE4 Alternate: TRACED1, TIMER0_BRKIN1, SAI0_DAT1, HPDF_DATAIN3, TIMER14_MCH0, SPI3_NSS, SAI0_FS0, SAI2_FS0, SAI2_DAT1, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT
PE5	4	I/O		Default: PE5 Alternate: TRACED2, SAI0_CLK1, HPDF_CKIN3, TIMER14_CH0 , SPI3_MISO, SAI0_SCK0, SAI2_SCK0, SAI2_CLK1, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT
PE6	5	I/O		Default: PE6 Alternate: TRACED3, TIMER0_BRKIN2, SAI0_DAT0, TIMER14_CH1 , SPI3_MOSI, SAI0_SD0 , SAI2_SD0, SAI2_DAT0, SAI1_MCLK1, CMP_MUX_OUT3 , EXMC_A22, DCI_D7, TLI_G1, EVENTOUT
VBAT	6	P	-	Default: VBAT
PC13	7	I/O		Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_TS, WKUP3, RTC_OUT
PC14-OSC32IN	8	I/O		Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O		Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PF0	10	I/O		Default: PF0 Alternate: I2C1_SDA, USBHS0_ULPI_D4, OSPIM_P1_IO0, EXMC_A0, TIMER22_CH0, EVENTOUT

LQFP144				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PF1	11	I/O		Default: PF1 Alternate: I2C1_SCL, USBHS0_ULPI_D5, OSPIM_P1_IO1, EXMC_A1, TIMER22_CH1, EVENTOUT
PF2	12	I/O		Default: PF2 Alternate: I2C1_SMBA, USBHS0_ULPI_D6, OSPIM_P1_IO2, EXMC_A2, TIMER22_CH2, EVENTOUT
PF3	13	I/O		Default: PF3 Alternate: OSPIM_P1_IO3, EXMC_A3, TIMER22_CH3, EVENTOUT Additional: ADC2_IN5
PF4	14	I/O		Default: PF4 Alternate: TIMER0_MCH1, TIMER7_MCH1, USART0_TX, HPDF_DATAIN2, USART2_RTS, USART2_DE, UART3_RTS, UART3_DE, OSPIM_P1_SCK, SDIO1_D0, EXMC_A4, TRIGSEL_OUT1, TLI_PIXCLK, EVENTOUT Additional: ADC2_IN9
PF5	15	I/O		Default: PF5 Alternate: TIMER0_MCH2, TIMER7_MCH2, USART0_RX, HPDF_CKIN2, UART3_CTS, SDIO1_D1, EXMC_A5, TRIGSEL_OUT5, TLI_G7, EVENTOUT Additional: ADC2_IN4
VSS	16	P	-	Default: VSS
VDD	17	P	-	Default: VDD
PF6	18	I/O		Default: PF6 Alternate: TIMER15_CH0, CAN2_RX, SPI4_NSS, SAI0_SD1, UART6_RX, SAI2_SD1, OSPIM_P0_IO3, EXMC_D24, TIMER22_CH0, EVENTOUT Additional: ADC2_IN8
PF7	19	I/O		Default: PF7 Alternate: TIMER16_CH0, CAN2_TX, SPI4_SCK, SAI0_MCLK1, UART6_TX, SAI2_MCLK1, OSPIM_P0_IO2, EXMC_D25, TIMER22_CH1, EVENTOUT Additional: ADC2_IN3
PF8	20	I/O		Default: PF8 Alternate: TIMER15_MCH0, SPI4_MISO, SAI0_SCK1, UART6_RTS, UART6_DE, SAI2_SCK1, OSPIM_P0_IO0, EXMC_D26, TIMER22_CH2, EVENTOUT Additional: ADC2_IN7
PF9	21	I/O		Default: PF9 Alternate: TIMER16_MCH0, SPI4_MOSI, SAI0_FS1, UART6_CTS, SAI2_FS1, OSPIM_P0_IO1, EXMC_D27, TIMER22_CH3, EVENTOUT Additional: ADC2_IN2
PF10	22	I/O		Default: PF10 Alternate: TIMER15_BRKIN0, SAI0_DAT2, OSPIM_P0_SCK,

LQFP144				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				SAI2_DAT2, DCI_D11, TLI_DE, EVENTOUT Additional: ADC2_IN6
PH0-OSCIN	23	I/O		Default: PH0 Alternate: EVENTOUT Additional: OSCIN
PH1-OSCOUT	24	I/O		Default: PH1 Alternate: EVENTOUT Additional: OSCOUT
NRST	25	-	-	Default: NRST
PC0	26	I/O		Default: PC0 Alternate: EXMC_D12, HPDF_CKIN0, HPDF_DATAIN4, TIMER40_CH0, SAI1_FS1, EXMC_A25, USBHS0_ULPI_STP, TLI_G2, EXMC_SDNWE, TRIGSEL_IN8, TLI_R5, EVENTOUT Additional: ADC012_IN10
PC1	27	I/O		Default: PC1 Alternate: TRACED0, SAI2_DAT0, SAI0_DAT0, HPDF_DATAIN0, HPDF_CKIN4, SPI1_MOSI, I2S1_SD, SAI0_SD0, TIMER40_MCH0, SAI2_SD0, SDIO1_CK, OSPIM_P0_IO4, ETH0_MDC, MDC, TRIGSEL_IN9, TLI_G5, EVENTOUT Additional: ADC012_IN11, RTC_TAMP2, WKUP5
PC2_C	28	I/O		Default: PC2_C(4) Additional: ADC2_IN0
PC3_C	29	I/O		Default: PC3_C(4) Additional: ADC2_IN1
VDD	30	P	-	Default: VDD
VSSA	31	P	-	Default: VSSA
VREFP	32	P	-	Default: VREFP
VDDA	33	P	-	Default: VDDA
PA0	34	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, TIMER14_BRKIN0, SPI5_NSS, I2S5_WS, OSPIM_P0_IO6, USART1_CTS, UART3_TX, SDIO1_CMD, SAI1_SD1, EXMC_A19, TRIGSEL_IN0 , EVENTOUT Additional: ADC0_IN16, WKUP0
PA1	35	I/O		Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, TIMER14_MCH0, USART1_RTS, USART1_DE, UART3_RX, OSPIM_P0_IO3, SAI1_MCLK1, ETH0_RMII_REF_CLK, TRIGSEL_IN1, TLI_R2, EVENTOUT Additional: ADC0_IN17
PA2	36	I/O		Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER14_CH0,

LQFP144				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				OSPIM_P0_IO0, USART1_TX, SAI1_SCK1, ETH0_MDIO, MDIO, TRIGSEL_IN7, TLI_R1, EVENTOUT Additional: ADC01_IN14, WKUP1
PA3	37	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER14_CH1, I2S5_MCK, OSPIM_P0_IO2, USART1_RX, TLI_B2, USBHS0_ULPI_D0, OSPIM_P0_SCK, TRIGSEL_IN4, TLI_B5, EVENTOUT Additional: ADC01_IN15
VSS	38	P	-	Default: VSS
VDD	39	P	-	Default: VDD
PA4	40	I/O		Default: PA4 Alternate: TIMER4_ETI, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, USART1_CK, SPI5_NSS, I2S5_WS, EXMC_D8, DCI_HSYNC, TLI_VSYNC, EVENTOUT Additional: ADC01_IN18, DAC0_OUT0
PA5	41	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_MCH0, SPI0_SCK, I2S0_CK, SPI5_SCK, I2S5_CK, USBHS0_ULPI_CK, MDIO_A0, EXMC_D9, TLI_R4, EVENTOUT Additional: ADC01_IN19, DAC0_OUT1
PA6	42	I/O		Default: PA6 Alternate: TIMER0_BRKIN0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, OSPIM_P0_IO3, SPI5_MISO, CMP_MUX_OUT0, MDIO_MDC, DCI_PIXCLK, TLI_G2, EVENTOUT Additional: ADC01_IN3
PA7	43	I/O		Default: PA7 Alternate: TIMER0_MCH0, TIMER2_CH1, TIMER7_MCH0, SPI0_MOSI, I2S0_SD, SPI5_MOSI, I2S5_SD, OSPIM_P0_IO2, ETH0_RMII_CRS_DV, EXMC_SDNWE, TRIGSEL_IN5, TLI_VSYNC, EVENTOUT Additional: ADC01_IN7
PC4	44	I/O		Default: PC4 Alternate: PMU_DEEPSLEEP, EXMC_A22, HPDF_CKIN2, I2S0_MCK, TIMER41_CH0, RSPDIF_CH2, SDIO1_CKIN, ETH0_RMII_RXD0, EXMC_SDNE0, TLI_R7, EVENTOUT Additional: ADC01_IN4, CMP0_IM7
PC5	45	I/O		Default: PC5 Alternate: PMU_SLEEP, SAI2_DAT2, SAI0_DAT2, HPDF_DATAIN2, TIMER41_MCH0, RSPDIF_CH3, ETH0_RMII_RXD1, EXMC_SDCKE0, CMP0_OUT, TLI_DE, EVENTOUT Additional: ADC01_IN8

LQFP144				
Pin Name	**Pins**	**Pin Type[(1)]**	**I/O Level[(2)]**	**Functions description**
PB0	46	I/O		Default: PB0 Alternate: TIMER0_MCH1, TIMER2_CH2, TIMER7_MCH1, OSPIM_P0_IO1, HPDF_CKOUT, UART3_CTS, TLI_R3, USBHS0_ULPI_D1, MDIO_A1, TRIGSEL_OUT3, TLI_G1, EVENTOUT Additional: ADC01_IN9, CMP0_IP0
PB1	47	I/O		Default: PB1 Alternate: TIMER0_MCH2, TIMER2_CH3, TIMER7_MCH2, OSPIM_P0_IO0, HPDF_DATAIN1, TLI_R6, USBHS0_ULPI_D2, MDIO_A2, TRIGSEL_OUT4, TLI_G0, EVENTOUT Additional: ADC01_IN5, CMP0_IM6
PB2	48	I/O		Default: PB2 Alternate: RTC_OUT, SAI2_DAT0, SAI0_DAT0, EXMC_D10, HPDF_CKIN1, SAI0_SD0, SPI2_MOSI, I2S2_SD, SAI2_SD0, OSPIM_P0_SCK, EXMC_NCE, MDIO_A3, TIMER22_ETI, EVENTOUT Additional: CMP0_IP1
PF11	49	I/O		Default: PF11 Alternate: SPI4_MOSI, SAI1_SD1, EXMC_SDNRAS, DCI_D12, TIMER23_CH0, EVENTOUT Additional: ADC0_IN2
PF12	50	I/O		Default: PF12 Alternate: EXMC_A6, TIMER23_CH1, EVENTOUT Additional: ADC0_IN6
VSS	51	P	-	Default: VSS
VDD	52	P	-	Default: VDD
PF13	53	I/O		Default: PF13 Alternate: HPDF_DATAIN6, I2C3_SMBA, EXMC_A7, TIMER23_CH2, EVENTOUT Additional: ADC1_IN2
PF14	54	I/O		Default: PF14 Alternate: HPDF_CKIN6, I2C3_SCL, SPI4_IO2, EXMC_A8, TIMER23_CH3, EVENTOUT Additional: ADC1_IN6
PF15	55	I/O		Default: PF15 Alternate: I2C3_SDA, SPI4_IO3, EXMC_A9, EVENTOUT
PG0	56	I/O		Default: PG0 Alternate: TIMER31_CH0, OSPIM_P1_IO4, EXMC_A10, EVENTOUT
PG1	57	I/O		Default: PG1 Alternate: TIMER31_CH1, OSPIM_P1_IO5, EXMC_A11, EVENTOUT
PE7	58	I/O		Default: PE7

LQFP144				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: TIMER0_ETI, HPDF_DATAIN2, UART6_RX, OSPIM_P0_IO4, EXMC_D4, EVENTOUT Additional: CMP1_IM7
PE8	59	I/O		Default: PE8 Alternate: TIMER0_MCH0, HPDF_CKIN2, UART6_TX, OSPIM_P0_IO5, EXMC_D5, CMP1_OUT, EVENTOUT
PE9	60	I/O		Default: PE9 Alternate: TIMER0_CH0, HPDF_CKOUT, SPI3_IO2, UART6_RTS, UART6_DE, OSPIM_P0_IO6, EXMC_D6, EVENTOUT Additional: CMP1_IP0
VSS	61	P	-	Default: VSS
VDD	62	P	-	Default: VDD
PE10	63	I/O		Default: PE10 Alternate: TIMER0_MCH1, HPDF_DATAIN4, SPI3_IO3, UART6_CTS, OSPIM_P0_IO7, EXMC_D7, EVENTOUT Additional: CMP1_IM6
PE11	64	I/O		Default: PE11 Alternate: TIMER0_CH1, HPDF_CKIN4, SPI3_NSS, SAI1_SD1, OSPIM_P0_CSN, EXMC_D8, TLI_G3, EVENTOUT Additional: CMP1_IP1
PE12	65	I/O		Default: PE12 Alternate: TIMER0_MCH2, HPDF_DATAIN5, SPI3_SCK, SAI1_SCK1, EXMC_D9, CMP0_OUT, TLI_B4, EVENTOUT
PE13	66	I/O		Default: PE13 Alternate: TIMER0_CH2, HPDF_CKIN5, SPI3_MISO, SAI1_FS1, EXMC_D10, CMP1_OUT, TLI_DE, EVENTOUT
PE14	67	I/O		Default: PE14 Alternate: TIMER0_CH3, SPI3_MOSI, SAI1_MCLK1, EXMC_D11, TLI_PIXCLK, EVENTOUT
PE15	68	I/O		Default: PE15 Alternate: TIMER0_BRKIN0, TLI_HSYNC, EXMC_D12, CMP_MUX_OUT4, TLI_R7, EVENTOUT
PB10	69	I/O		Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, HPDF_DATAIN7, USART2_TX, OSPIM_P0_CSN, USBHS0_ULPI_D3, TRIGSEL_OUT2, TLI_G4, EVENTOUT
PB11	70	I/O		Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, HPDF_CKIN7, USART2_RX, USBHS0_ULPI_D4, ETH0_RMII_TX_EN, TLI_G5, EVENTOUT
VCORE	71	P	-	Default: VCORE
VDD	72	P	-	Default: VDD

LQFP144				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PB12	73	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN0, I2C1_SMBA, SPI1_NSS, I2S1_WS, HPDF_DATAIN1, USART2_CK, CAN1_RX, USBHS0_ULPI_D5, ETH0_RMII_TXD0, OSPIM_P0_IO0, CMP_MUX_OUT2, UART4_RX, EVENTOUT
PB13	74	I/O	5VT	Default: PB13 Alternate: RTC_REFIN, TIMER0_MCH0, OSPIM_P0_IO2, SPI1_SCK, I2S1_CK, HPDF_CKIN1, USART2_CTS, CAN1_TX, USBHS0_ULPI_D6, ETH0_RMII_TXD1, SDIO0_D0, DCI_D2, UART4_TX, EVENTOUT
PB14	75	I/O		Default: PB14 Alternate: TIMER0_MCH1, TIMER7_MCH1, USART0_TX, SPI1_MISO, HPDF_DATAIN2, USART2_RTS, USART2_DE, UART3_RTS, UART3_DE, SDIO1_D0, EXMC_D10, TRIGSEL_OUT1, TLI_PIXCLK, EVENTOUT
PB15	76	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER0_MCH2, TIMER7_MCH2, USART0_RX, SPI1_MOSI, I2S1_SD, HPDF_CKIN2, UART3_CTS, SDIO1_D1, EXMC_D11, TRIGSEL_OUT5, TLI_G7, EVENTOUT
PD8	77	I/O		Default: PD8 Alternate: HPDF_CKIN3, USART2_TX, SAI1_CLK0, RSPDIF_CH1, EXMC_D13, EVENTOUT
PD9	78	I/O		Default: PD9 Alternate: HPDF_DATAIN3, USART2_RX, SAI1_CLK1, EXMC_D14, EVENTOUT
PD10	79	I/O		Default: PD10 Alternate: HPDF_CKOUT, USART2_CK, SAI1_DAT1, EXMC_D15, TLI_B3, EVENTOUT
PD11	80	I/O		Default: PD11 Alternate: TIMER40_CH1, TIMER7_MCH3, I2C3_SMBA, USART2_CTS, SAI1_DAT2, OSPIM_P0_IO0, SAI1_SD0, EXMC_A16, EXMC_CLE, EVENTOUT
PD12	81	I/O		Default: PD12 Alternate: TIMER41_CH1, TIMER3_CH0, I2C3_SCL, CAN2_RX, EDOUT_A, USART2_RTS, USART2_DE, OSPIM_P0_IO1, SAI1_FS0, EXMC_A17, EXMC_ALE, DCI_D12, EVENTOUT
PD13	82	I/O		Default: PD13 Alternate: TIMER42_CH1, TIMER3_CH1, I2C3_SDA, CAN2_TX, EDOUT_B, OSPIM_P0_IO3, SAI1_SCK0, EXMC_A18, DCI_D13, EVENTOUT
VSS	83	P	-	Default: VSS
VDD	84	P	-	Default: VDD
PD14	85	I/O		Default: PD14

LQFP144				
Pin Name	Pins	Pin Type[1]	I/O Level[2]	Functions description
				Alternate: TIMER43_CH1, TIMER3_CH2, SPI3_IO2, EDOUT_Z, UART7_CTS, EXMC_D0, EVENTOUT
PD15	86	I/O		Default: PD15 Alternate: TIMER44_CH1, TIMER3_CH3, SPI3_IO3, UART7_RTS, UART7_DE, EXMC_D1, EVENTOUT
PG2	87	I/O		Default: PG2 Alternate: TIMER0_BRKIN1, TIMER7_BRKIN0, TIMER31_CH2, SPI1_MISO, CMP_MUX_OUT5, EXMC_A12, TIMER23_ETI, EVENTOUT
PG3	88	I/O		Default: PG3 Alternate: TIMER7_BRKIN2, TIMER31_CH3, SPI1_MOSI, I2S1_SD, CMP_MUX_OUT6, EXMC_A13, TIMER22_ETI, EVENTOUT
PG4	89	I/O		Default: PG4 Alternate: TIMER0_BRKIN2, TIMER7_BRKIN1, TIMER31_ETI, CMP_MUX_OUT7, EXMC_A14, EVENTOUT
PG5	90	I/O		Default: PG5 Alternate: TIMER0_ETI, TIMER30_CH0, EXMC_A15, EVENTOUT
PG6	91	I/O		Default: PG6 Alternate: TIMER16_BRKIN0, TIMER30_CH1, OSPIM_P0_CSN, EXMC_NE2, DCI_D12, TLI_R7, EVENTOUT
PG7	92	I/O		Default: PG7 Alternate: EXMC_D28, TIMER30_CH2, SAI0_MCLK0, USART5_CK, EXMC_INT, DCI_D13, TLI_PIXCLK, EVENTOUT
PG8	93	I/O		Default: PG8 Alternate: TIMER7_ETI, TIMER30_CH3, SPI5_NSS, I2S5_WS, USART5_RTS, USART5_DE, RSPDIF_CH2, ETH0_PPS_OUT, EXMC_SDCLK, TLI_G7, EVENTOUT
VSS	94	P	-	Default: VSS
VDD33USB	95	P	-	Default: VDD33USB
PC6	96	I/O		Default: PC6 Alternate: TIMER0_BRKIN1, TIMER2_CH0, TIMER7_CH0, HPDF_CKIN3, I2S1_MCK, USART5_TX, SDIO0_DAT0DIR, EXMC_NWAIT, SDIO1_D6, SDIO0_D6, DCI_D0, TLI_HSYNC, EVENTOUT
PC7	97	I/O		Default: PC7 Alternate: TIMER0_CH3, TIMER2_CH1, TIMER7_CH1, HPDF_DATAIN3, I2S2_MCK, USART5_RX, SDIO0_DAT123DIR, EXMC_NE0, SDIO1_D7, SDIO0_D7, DCI_D1, TLI_G6, EVENTOUT
PC8	98	I/O		Default: PC8

LQFP144				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: TRACED1, TIMER2_CH2, TIMER7_CH2, USART5_CK, UART4_RTS, UART4_DE, EXMC_NE1, EXMC_INT, SDIO0_D0, DCI_D2, EVENTOUT
PC9	99	I/O		Default: PC9 Alternate: CK_OUT1, TIMER0_MCH3, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, UART4_CTS, OSPIM_P0_IO0, TLI_G3, SDIO0_D1, DCI_D3, TLI_B2, EVENTOUT
PA8	100	I/O		Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, TIMER7_BRKIN2, I2C2_SCL, USART0_CK, USBHS0_SOF, UART6_RX, CMP_MUX_OUT1, TLI_B3, TLI_R6, EVENTOUT
PA9	101	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, TRIGSEL_IN13, DCI_D0, TLI_R5, EVENTOUT Additional: USBHS0_VBUS
PA10	102	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, USART0_RX, TRIGSEL_IN12, USBHS0_ID, MDIO, TLI_B4, DCI_D1, TLI_B1, EVENTOUT
USBHS0_DM	103	I/O		Default: USBHS0_DM(3)
USBHS0_DP	104	I/O		Default: USBHS0_DP(3)
PA13	105	I/O		Default: JTMS, SWDIO, PA13 Alternate: TIMER0_BRKIN1, TIMER7_BRKIN1, SPI1_NSS, I2S1_WS, UART3_RX, USART0_CTS, CAN0_RX, MDIO_A3, EXMC_INT, TRIGSEL_IN10, TLI_R4, EVENTOUT
VCORE	106	P	-	Default: VCORE
VSS	107	P	-	Default: VSS
VDD	108	P	-	Default: VDD
PA14	109	I/O		Default: JTCK, SWCLK, PA14 Alternate: TLI_G7, SPI1_SCK, I2S1_CK, UART3_TX, USART0_RTS, USART0_DE, SAI1_FS1, CAN0_TX, MDIO_A4, TIMER0_BRKIN2, TRIGSEL_IN11, TLI_R5, EVENTOUT
PA15	110	I/O		Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, SPI5_NSS, I2S5_WS, UART3_RTS, UART3_DE, TLI_R3, UART6_TX, MDIO_A0, TRIGSEL_OUT0, TLI_B6, EVENTOUT
PC10	111	I/O		Default: PC10 Alternate: TIMER0_CH3, HPDF_CKIN5, SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, OSPIM_P0_IO1,

LQFP144				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TLI_B1, MDIO_A1, SDIO0_D2, DCI_D8, TLI_R2, EVENTOUT
PC11	112	I/O		Default: PC11 Alternate: TIMER0_ETI, HPDF_DATAIN5, SPI2_MISO, USART2_RX, UART3_RX, OSPIM_P0_CSN, EXMC_NBL2, MDIO_A2, SDIO0_D3, DCI_D4, TLI_B4, EVENTOUT
PC12	113	I/O		Default: PC12 Alternate: TRACED3, EXMC_D6, TIMER14_CH0, SPI5_SCK, I2S5_CK, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO0_CK, DCI_D9, TLI_R6, EVENTOUT
PD0	114	I/O		Default: PD0 Alternate: TIMER7_CH2, HPDF_CKIN6, UART3_RX, CAN0_RX, EXMC_D2, TRIGSEL_IN3, TLI_B1, EVENTOUT
PD1	115	I/O		Default: PD1 Alternate: HPDF_DATAIN6, UART3_TX, CAN0_TX, EXMC_D3, TRIGSEL_IN6, EVENTOUT
PD2	116	I/O		Default: PD2 Alternate: TRACED2, EXMC_D7, TIMER2_ETI, TIMER14_BRKIN0, UART4_RX, TLI_B7, SDIO0_CMD, DCI_D11, TLI_B2, EVENTOUT
PD3	117	I/O		Default: PD3 Alternate: HPDF_CKOUT, SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT
PD4	118	I/O		Default: PD4 Alternate: TIMER7_MCH3, USART1_RTS, USART1_DE, OSPIM_P0_IO4, EXMC_NOE, EVENTOUT
PD5	119	I/O		Default: PD5 Alternate: TIMER7_CH3, USART1_TX, OSPIM_P0_IO5, EXMC_NWE, EVENTOUT
VSS	120	P	-	Default: VSS
VDD	121	P	-	Default: VDD
PD6	122	I/O		Default: PD6 Alternate: SAI1_DAT0, SAI0_DAT0, HPDF_CKIN4, HPDF_DATAIN1, SPI2_MOSI, I2S2_SD, SAI0_SD0, USART1_RX, SAI2_SD0, OSPIM_P0_IO6, SDIO1_CK, EXMC_NWAIT, DCI_D10, TLI_B2, EVENTOUT
PD7	123	I/O		Default: PD7 Alternate: HPDF_DATAIN4, SPI0_MOSI, I2S0_SD, HPDF_CKIN1, USART1_CK, RSPDIF_CH0, OSPIM_P0_IO7, SDIO1_CMD, EXMC_NE0, EXMC_NCE, EVENTOUT
PG9	124	I/O		Default: PG9 Alternate: EXMC_D30, CAN2_TX, TIMER7_BRKIN1, TIMER30_ETI, SPI0_MISO, USART5_RX, RSPDIF_CH3,

LQFP144				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				OSPIM_P0_IO6, SAI1_FS1, SDIO1_D0, EXMC_NE1, DCI_VSYNC, EVENTOUT
PG10	125	I/O		Default: PG10 Alternate: EXMC_D31, CAN2_RX, OSPIM_P1_IO6, SPI0_NSS, I2S0_WS, TLI_G3, SAI1_SD1, SDIO1_D1, EXMC_NE2, DCI_D2, TLI_B2, EVENTOUT
PG11	126	I/O		Default: PG11 Alternate: EXMC_D29, SPI0_SCK, I2S0_CK, RSPDIF_CH0, OSPIM_P1_IO7, SDIO1_D2, ETH0_RMII_TX_EN, DCI_D3, TLI_B3, EVENTOUT
PG12	127	I/O		Default: PG12 Alternate: OSPIM_P1_CSN, SPI5_MISO, USART5_RTS, USART5_DE, RSPDIF_CH1, TLI_B4, SDIO1_D3, ETH0_RMII_TXD1, EXMC_NE3, TIMER22_CH0, TLI_B1, EVENTOUT
PG13	128	I/O		Default: PG13 Alternate: TRACED0, SPI5_SCK, I2S5_CK, USART5_CTS, TIMER44_CH0, SDIO1_D6, ETH0_RMII_TXD0, EXMC_A24, TIMER22_CH1, TLI_R0, EVENTOUT
PG14	129	I/O		Default: PG14 Alternate: TRACED1, SPI5_MOSI, I2S5_SD, USART5_TX, TIMER44_MCH0, OSPIM_P0_IO7, SDIO1_D7, ETH0_RMII_TXD1, EXMC_A25, TIMER22_CH2, TLI_B0, EVENTOUT
VSS	130	P	-	Default: VSS
VDD	131	P	-	Default: VDD
PG15	132	I/O		Default: PG15 Alternate: USART5_CTS, TIMER44_BRKIN0, EXMC_SDNCAS, DCI_D13, EVENTOUT
PB3	133	I/O		Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, TLI_PIXCLK, SPI0_SCK, I2S0_CK, SPI2_SCK, I2S2_CK, SPI5_SCK, I2S5_CK, SDIO1_D2, CTC_SYNC, UART6_RX, MDIO_A4, TRIGSEL_OUT7, TIMER23_ETI, EVENTOUT
PB4	134	I/O		Default: NJTRST, PB4 Alternate: TIMER15_BRKIN0, TIMER2_CH0, SPI0_MISO, SPI2_MISO, SPI1_NSS, I2S1_WS, SPI5_MISO, SDIO1_D3, UART6_TX, TRIGSEL_OUT6, EVENTOUT
PB5	135	I/O		Default: PB5 Alternate: TIMER16_BRKIN0, TIMER2_CH1, TLI_B5, I2C0_SMBA, SPI0_MOSI, I2S0_SD, I2C3_SMBA, SPI2_MOSI, I2S2_SD, SPI5_MOSI, I2S5_SD, CAN1_RX, USBHS0_ULPI_D7, ETH0_PPS_OUT, EXMC_SDCKE1, DCI_D10, UART4_RX, EVENTOUT
PB6	136	I/O		Default: PB6

LQFP144				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				Alternate: TIMER15_MCH0, TIMER3_CH0, EXMC_D11, I2C0_SCL, I2C3_SCL, USART0_TX, CAN1_TX, OSPIM_P0_CSN, HPDF_DATAIN5, EXMC_SDNE1, DCI_D5, UART4_TX, EVENTOUT
PB7	137	I/O		Default: PB7 Alternate: TIMER16_MCH0, TIMER3_CH1, I2C0_SDA, I2C3_SDA, USART0_RX, HPDF_CKIN5, EXMC_NL, EXMC_NADV, DCI_VSYNC, EVENTOUT Additional: PVD_IN
BOOT	138	I/O		Default: BOOT
PB8	139	I/O		Default: PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, I2C3_SCL, SDIO0_CKIN, UART3_RX, CAN0_RX, SDIO1_D4, SDIO0_D4, DCI_D6, TLI_B6, EVENTOUT
PB9	140	I/O		Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, SPI1_NSS, I2S1_WS, I2C3_SDA, SDIO0_CMDDIR, UART3_TX, CAN0_TX, SDIO1_D5, I2C3_SMBA, SDIO0_D5, DCI_D7, TLI_B7, EVENTOUT
PE0	141	I/O		Default: PE0 Alternate: TIMER3_ETI, UART7_RX, SAI1_MCLK0, EXMC_NBL0, DCI_D2, TLI_R0, EVENTOUT
PE1	142	I/O		Default: PE1 Alternate: UART7_TX, EXMC_NBL1, DCI_D3, TLI_R6, EVENTOUT
PDR_ON	143	P	-	Default: PDR_ON(5)
VDD	144	P	-	Default: VDD

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) USBHS0_DM and USBHS0_DP pins can only be used for USBHS.

(4) PC2_C and PC3_C can only be used as analog pins.

(5) PDR_ON pin should be pulled up to V_{DD}, refer to ***Figure 4-2. Recommended PDR_ON pin circuit(1)***.

2.6.2. GD32H757Vx LQFP100 pin definitions

Table 2-4. GD32H757Vx LQFP100 pin definitions

LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
PE2	1	I/O		Default: PE2 Alternate: TRACECK, SAI0_CLK0, SPI3_SCK, SAI0_MCLK0, OSPIM_P0_IO2, EXMC_A23, EVENTOUT
PE3	2	I/O		Default: PE3 Alternate: TRACED0, TIMER14_BRKIN0, SAI0_SD1, EXMC_A19, DCI_PIXCLK, EVENTOUT
PE4	3	I/O		Default: PE4 Alternate: TRACED1, TIMER0_BRKIN1, SAI0_DAT1, HPDF_DATAIN3, TIMER14_MCH0, SPI3_NSS, SAI0_FS0, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT
PE5	4	I/O		Default: PE5 Alternate: TRACED2, SAI0_CLK1, HPDF_CKIN3, TIMER14_CH0 , SPI3_MISO, SAI0_SCK0, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT
PE6	5	I/O		Default: PE6 Alternate: TRACED3, TIMER0_BRKIN2, SAI0_DAT0, TIMER14_CH1 , SPI3_MOSI, SAI0_SD0 , SAI1_MCLK1, CMP_MUX_OUT3, EXMC_A22, DCI_D7, TLI_G1, EVENTOUT
VBAT	6	P	-	Default: VBAT
PC13	7	I/O		Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_TS, WKUP3, RTC_OUT
PC14-OSC32IN	8	I/O		Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	9	I/O		Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
VSS	10	P	-	Default: VSS
VDD	11	P	-	Default: VDD
PH0-OSCIN	12	I/O		Default: PH0 Alternate: EVENTOUT Additional: OSCIN
PH1-OSCOUT	13	I/O		Default: PH1 Alternate: EVENTOUT Additional: OSCOUT
NRST	14	-	-	Default: NRST
PC0	15	I/O		Default: PC0 Alternate: EXMC_D12, HPDF_CKIN0, HPDF_DATAIN4, TIMER40_CH0, SAI1_FS1, EXMC_A25,

LQFP100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				USBHS0_ULPI_STP, TLI_G2, EXMC_SDNWE, TRIGSEL_IN8, TLI_R5, EVENTOUT Additional: ADC012_IN10
PC1	16	I/O		Default: PC1 Alternate: TRACED0, SAI0_DAT0, HPDF_DATAIN0, HPDF_CKIN4, SPI1_MOSI, I2S1_SD, SAI0_SD0, TIMER40_MCH0, SDIO1_CK, OSPIM_P0_IO4, ETH0_MDC, MDC, TRIGSEL_IN9, TLI_G5, EVENTOUT Additional: ADC012_IN11, RTC_TAMP2, WKUP5
PC2_C	17	I/O		Default: PC2_C(4) Additional: ADC2_IN0
PC3_C	18	I/O		Default: PC3_C(4) Additional: ADC2_IN1
VSSA	19	P	-	Default: VSSA
VREFP	20	P	-	Default: VREFP
VDDA	21	P	-	Default: VDDA
PA0	22	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, TIMER14_BRKIN0, SPI5_NSS, I2S5_WS, OSPIM_P0_IO6, USART1_CTS, UART3_TX, SDIO1_CMD, SAI1_SD1, EXMC_A19, TRIGSEL_IN0 , EVENTOUT Additional: ADC0_IN16, WKUP0
PA1	23	I/O		Default: PA1 Alternate: TIMER1_CH1, TIMER4_CH1, TIMER14_MCH0, USART1_RTS, USART1_DE, UART3_RX, OSPIM_P0_IO3, SAI1_MCLK1, ETH0_RMII_REF_CLK, TRIGSEL_IN1, TLI_R2, EVENTOUT Additional: ADC0_IN17
PA2	24	I/O		Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER14_CH0, OSPIM_P0_IO0, USART1_TX, SAI1_SCK1, ETH0_MDIO, MDIO, TRIGSEL_IN7 , TLI_R1, EVENTOUT Additional: ADC01_IN14, WKUP1
PA3	25	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER14_CH1, I2S5_MCK, OSPIM_P0_IO2, USART1_RX, TLI_B2, USBHS0_ULPI_D0, OSPIM_P0_SCK, TRIGSEL_IN4, TLI_B5, EVENTOUT Additional: ADC01_IN15
VSS	26	P	-	Default: VSS
VDD	27	P	-	Default: VDD
PA4	28	I/O		Default: PA4

LQFP100				
Pin Name	Pins	Pin Type[(1)]	I/O Level[(2)]	Functions description
				Alternate: TIMER4_ETI, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, USART1_CK, SPI5_NSS, I2S5_WS, EXMC_D8, DCI_HSYNC, TLI_VSYNC, EVENTOUT Additional: ADC01_IN18, DAC0_OUT0
PA5	29	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_MCH0, SPI0_SCK, I2S0_CK, SPI5_SCK, I2S5_CK, USBHS0_ULPI_CK, MDIO_A0, EXMC_D9, TLI_R4, EVENTOUT Additional: ADC01_IN19, DAC0_OUT1
PA6	30	I/O		Default: PA6 Alternate: TIMER0_BRKIN0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, OSPIM_P0_IO3, SPI5_MISO, CMP_MUX_OUT0, MDIO_MDC, DCI_PIXCLK, TLI_G2, EVENTOUT Additional: ADC01_IN3
PA7	31	I/O		Default: PA7 Alternate: TIMER0_MCH0, TIMER2_CH1, TIMER7_MCH0, SPI0_MOSI, I2S0_SD, SPI5_MOSI, I2S5_SD, OSPIM_P0_IO2, ETH0_RMII_CRS_DV, EXMC_SDNWE, TRIGSEL_IN5, TLI_VSYNC, EVENTOUT Additional: ADC01_IN7
PC4	32	I/O		Default: PC4 Alternate: PMU_DEEPSLEEP, EXMC_A22, HPDF_CKIN2, I2S0_MCK, TIMER41_CH0, RSPDIF_CH2, SDIO1_CKIN, ETH0_RMII_RXD0, EXMC_SDNE0, TLI_R7, EVENTOUT Additional: ADC01_IN4, CMP0_IM7
PC5	33	I/O		Default: PC5 Alternate: PMU_SLEEP, SAI0_DAT2, HPDF_DATAIN2, TIMER41_MCH0, RSPDIF_CH3, ETH0_RMII_RXD1, EXMC_SDCKE0, CMP0_OUT, TLI_DE, EVENTOUT Additional: ADC01_IN8
PB0	34	I/O		Default: PB0 Alternate: TIMER0_MCH1, TIMER2_CH2, TIMER7_MCH1, OSPIM_P0_IO1, HPDF_CKOUT, UART3_CTS, TLI_R3, USBHS0_ULPI_D1, MDIO_A1, TRIGSEL_OUT3, TLI_G1, EVENTOUT Additional: ADC01_IN9, CMP0_IP0
PB1	35	I/O		Default: PB1 Alternate: TIMER0_MCH2, TIMER2_CH3, TIMER7_MCH2, OSPIM_P0_IO0, HPDF_DATAIN1, TLI_R6, USBHS0_ULPI_D2, MDIO_A2, TRIGSEL_OUT4, TLI_G0, EVENTOUT Additional: ADC01_IN5, CMP0_IM6
PB2	36	I/O		Default: PB2

LQFP100				
Pin Name	Pins	Pin Type[(1)]	I/O Level[(2)]	Functions description
				Alternate: RTC_OUT, SAI0_DAT0, EXMC_D10, HPDF_CKIN1, SAI0_SD0, SPI2_MOSI, I2S2_SD, OSPIM_P0_SCK, EXMC_NCE, MDIO_A3, TIMER22_ETI, EVENTOUT Additional: CMP0_IP1
PE7	37	I/O		Default: PE7 Alternate: TIMER0_ETI, HPDF_DATAIN2, UART6_RX, OSPIM_P0_IO4, EXMC_D4, EVENTOUT Additional: CMP1_IM7
PE8	38	I/O		Default: PE8 Alternate: TIMER0_MCH0, HPDF_CKIN2, UART6_TX, OSPIM_P0_IO5, EXMC_D5, CMP1_OUT, EVENTOUT
PE9	39	I/O		Default: PE9 Alternate: TIMER0_CH0, HPDF_CKOUT, SPI3_IO2, UART6_RTS, UART6_DE, OSPIM_P0_IO6, EXMC_D6, EVENTOUT Additional: CMP1_IP0
PE10	40	I/O		Default: PE10 Alternate: TIMER0_MCH1, HPDF_DATAIN4, SPI3_IO3, UART6_CTS, OSPIM_P0_IO7, EXMC_D7, EVENTOUT Additional: CMP1_IM6
PE11	41	I/O		Default: PE11 Alternate: TIMER0_CH1, HPDF_CKIN4, SPI3_NSS, SAI1_SD1, OSPIM_P0_CSN, EXMC_D8, TLI_G3, EVENTOUT Additional: CMP1_IP1
PE12	42	I/O		Default: PE12 Alternate: TIMER0_MCH2, HPDF_DATAIN5, SPI3_SCK, SAI1_SCK1, EXMC_D9, CMP0_OUT, TLI_B4, EVENTOUT
PE13	43	I/O		Default: PE13 Alternate: TIMER0_CH2, HPDF_CKIN5, SPI3_MISO, SAI1_FS1, EXMC_D10, CMP1_OUT, TLI_DE, EVENTOUT
PE14	44	I/O		Default: PE14 Alternate: TIMER0_CH3, SPI3_MOSI, SAI1_MCLK1, EXMC_D11, TLI_PIXCLK, EVENTOUT
PE15	45	I/O		Default: PE15 Alternate: TIMER0_BRKIN0, TLI_HSYNC, EXMC_D12, CMP_MUX_OUT4, TLI_R7, EVENTOUT
PB10	46	I/O		Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, HPDF_DATAIN7, USART2_TX, OSPIM_P0_CSN, USBHS0_ULPI_D3, TRIGSEL_OUT2, TLI_G4, EVENTOUT
PB11	47	I/O		Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, HPDF_CKIN7, USART2_RX, USBHS0_ULPI_D4, ETH0_RMII_TX_EN,

LQFP100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				TLI_G5, EVENTOUT
VCORE	48	P	-	Default: VCORE
VSS	49	P	-	Default: VSS
VDD	50	P	-	Default: VDD
PB12	51	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN0, I2C1_SMBA, SPI1_NSS, I2S1_WS, HPDF_DATAIN1, USART2_CK, CAN1_RX, USBHS0_ULPI_D5, ETH0_RMII_TXD0, OSPIM_P0_IO0, CMP_MUX_OUT2, UART4_RX, EVENTOUT
PB13	52	I/O	5VT	Default: PB13 Alternate: RTC_REFIN, TIMER0_MCH0, OSPIM_P0_IO2, SPI1_SCK, I2S1_CK, HPDF_CKIN1, USART2_CTS, CAN1_TX, USBHS0_ULPI_D6, ETH0_RMII_TXD1, SDIO0_D0, DCI_D2, UART4_TX, EVENTOUT
PB14	53	I/O		Default: PB14 Alternate: TIMER0_MCH1, TIMER7_MCH1, USART0_TX, SPI1_MISO, HPDF_DATAIN2, USART2_RTS, USART2_DE, UART3_RTS, UART3_DE, SDIO1_D0, EXMC_D10, TRIGSEL_OUT1, TLI_PIXCLK, EVENTOUT
PB15	54	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER0_MCH2, TIMER7_MCH2, USART0_RX, SPI1_MOSI, I2S1_SD, HPDF_CKIN2, UART3_CTS, SDIO1_D1, EXMC_D11, TRIGSEL_OUT5, TLI_G7, EVENTOUT
PD8	55	I/O		Default: PD8 Alternate: HPDF_CKIN3, USART2_TX, SAI1_CLK0, RSPDIF_CH1, EXMC_D13, EVENTOUT
PD9	56	I/O		Default: PD9 Alternate: HPDF_DATAIN3, USART2_RX, SAI1_CLK1, EXMC_D14, EVENTOUT
PD10	57	I/O		Default: PD10 Alternate: HPDF_CKOUT, USART2_CK, SAI1_DAT1, EXMC_D15, TLI_B3, EVENTOUT
PD11	58	I/O		Default: PD11 Alternate: TIMER40_CH1, TIMER7_MCH3, I2C3_SMBA, USART2_CTS, SAI1_DAT2, OSPIM_P0_IO0, SAI1_SD0, EXMC_A16, EXMC_CLE, EVENTOUT
PD12	59	I/O		Default: PD12 Alternate: TIMER41_CH1, TIMER3_CH0, I2C3_SCL, CAN2_RX, EDOUT_A, USART2_RTS, USART2_DE, OSPIM_P0_IO1, SAI1_FS0, EXMC_A17, EXMC_ALE, DCI_D12, EVENTOUT
PD13	60	I/O		Default: PD13 Alternate: TIMER42_CH1, TIMER3_CH1, I2C3_SDA, CAN2_TX, EDOUT_B, OSPIM_P0_IO3, SAI1_SCK0,

LQFP100				
Pin Name	**Pins**	**Pin Type(1)**	**I/O Level(2)**	**Functions description**
				EXMC_A18, DCI_D13, EVENTOUT
PD14	61	I/O		Default: PD14 Alternate: TIMER43_CH1, TIMER3_CH2, SPI3_IO2, EDOUT_Z, UART7_CTS, EXMC_D0, EVENTOUT
PD15	62	I/O		Default: PD15 Alternate: TIMER44_CH1, TIMER3_CH3, SPI3_IO3, UART7_RTS, UART7_DE, EXMC_D1, EVENTOUT
PC6	63	I/O		Default: PC6 Alternate: TIMER0_BRKIN1, TIMER2_CH0, TIMER7_CH0, HPDF_CKIN3, I2S1_MCK, USART5_TX, SDIO0_DAT0DIR, EXMC_NWAIT, SDIO1_D6, SDIO0_D6, DCI_D0, TLI_HSYNC, EVENTOUT
PC7	64	I/O		Default: PC7 Alternate: TIMER0_CH3, TIMER2_CH1, TIMER7_CH1, HPDF_DATAIN3, I2S2_MCK, USART5_RX, SDIO0_DAT123DIR, EXMC_NE0, SDIO1_D7, SDIO0_D7, DCI_D1, TLI_G6, EVENTOUT
PC8	65	I/O		Default: PC8 Alternate: TRACED1, TIMER2_CH2, TIMER7_CH2, USART5_CK, UART4_RTS, UART4_DE, EXMC_NE1, EXMC_INT, SDIO0_D0, DCI_D2, EVENTOUT
PC9	66	I/O		Default: PC9 Alternate: CK_OUT1, TIMER0_MCH3, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, UART4_CTS, OSPIM_P0_IO0, TLI_G3, SDIO0_D1, DCI_D3, TLI_B2, EVENTOUT
PA8	67	I/O		Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, TIMER7_BRKIN2, I2C2_SCL, USART0_CK, USBHS0_SOF, UART6_RX, CMP_MUX_OUT1, TLI_B3, TLI_R6, EVENTOUT
PA9	68	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, TRIGSEL_IN13, DCI_D0, TLI_R5, EVENTOUT Additional: USBHS0_VBUS
PA10	69	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, USART0_RX, TRIGSEL_IN12, USBHS0_ID, MDIO, TLI_B4, DCI_D1, TLI_B1, EVENTOUT
USBHS0_DM	70	I/O		Default: USBHS0_DM(3)
USBHS0_DP	71	I/O		Default: USBHS0_DP(3)
PA13	72	I/O		Default: JTMS, SWDIO, PA13 Alternate: TIMER0_BRKIN1, TIMER7_BRKIN1, SPI1_NSS, I2S1_WS, UART3_RX, USART0_CTS, CAN0_RX, MDIO_A3, EXMC_INT, TRIGSEL_IN10, TLI_R4,

LQFP100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				EVENTOUT
VCORE	73	P	-	Default: VCORE
VSS	74	P	-	Default: VSS
VDD	75	P	-	Default: VDD
PA14	76	I/O		Default: JTCK, SWCLK, PA14 Alternate: TLI_G7, SPI1_SCK, I2S1_CK, UART3_TX, USART0_RTS, USART0_DE, SAI1_FS1, CAN0_TX, MDIO_A4, TIMER0_BRKIN2, TRIGSEL_IN11, TLI_R5, EVENTOUT
PA15	77	I/O		Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, SPI5_NSS, I2S5_WS, UART3_RTS, UART3_DE, TLI_R3, UART6_TX, MDIO_A0, TRIGSEL_OUT0, TLI_B6, EVENTOUT
PC10	78	I/O		Default: PC10 Alternate: TIMER0_CH3, HPDF_CKIN5, SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, OSPIM_P0_IO1, TLI_B1, MDIO_A1, SDIO0_D2, DCI_D8, TLI_R2, EVENTOUT
PC11	79	I/O		Default: PC11 Alternate: TIMER0_ETI, HPDF_DATAIN5, SPI2_MISO, USART2_RX, UART3_RX, OSPIM_P0_CSN, EXMC_NBL2, MDIO_A2, SDIO0_D3, DCI_D4, TLI_B4, EVENTOUT
PC12	80	I/O		Default: PC12 Alternate: TRACED3, EXMC_D6, TIMER14_CH0, SPI5_SCK, I2S5_CK, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO0_CK, DCI_D9, TLI_R6, EVENTOUT
PD0	81	I/O		Default: PD0 Alternate: TIMER7_CH2, HPDF_CKIN6, UART3_RX, CAN0_RX, EXMC_D2, TRIGSEL_IN3, TLI_B1, EVENTOUT
PD1	82	I/O		Default: PD1 Alternate: HPDF_DATAIN6, UART3_TX, CAN0_TX, EXMC_D3, TRIGSEL_IN6, EVENTOUT
PD2	83	I/O		Default: PD2 Alternate: TRACED2, EXMC_D7, TIMER2_ETI, TIMER14_BRKIN0, UART4_RX, TLI_B7, SDIO0_CMD, DCI_D11, TLI_B2, EVENTOUT
PD3	84	I/O		Default: PD3 Alternate: HPDF_CKOUT, SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT
PD4	85	I/O		Default: PD4 Alternate: TIMER7_MCH3, USART1_RTS, USART1_DE, OSPIM_P0_IO4, EXMC_NOE, EVENTOUT
PD5	86	I/O		Default: PD5 Alternate: TIMER7_CH3, USART1_TX, OSPIM_P0_IO5,

LQFP100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				EXMC_NWE, EVENTOUT
PD6	87	I/O		Default: PD6 Alternate: SAI1_DAT0, SAI0_DAT0, HPDF_CKIN4, HPDF_DATAIN1, SPI2_MOSI, I2S2_SD, SAI0_SD0, USART1_RX, OSPIM_P0_IO6, SDIO1_CK, EXMC_NWAIT, DCI_D10, TLI_B2, EVENTOUT
PD7	88	I/O		Default: PD7 Alternate: HPDF_DATAIN4, SPI0_MOSI, I2S0_SD, HPDF_CKIN1, USART1_CK, RSPDIF_CH0, OSPIM_P0_IO7, SDIO1_CMD, EXMC_NE0, EXMC_NCE, EVENTOUT
PB3	89	I/O		Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, TLI_PIXCLK, SPI0_SCK, I2S0_CK, SPI2_SCK, I2S2_CK, SPI5_SCK, I2S5_CK, SDIO1_D2, CTC_SYNC, UART6_RX, MDIO_A4, TRIGSEL_OUT7, TIMER23_ETI, EVENTOUT
PB4	90	I/O		Default: NJTRST, PB4 Alternate: TIMER15_BRKIN0, TIMER2_CH0, SPI0_MISO, SPI2_MISO, SPI1_NSS, I2S1_WS, SPI5_MISO, SDIO1_D3, UART6_TX, TRIGSEL_OUT6, EVENTOUT
PB5	91	I/O		Default: PB5 Alternate: TIMER16_BRKIN0, TIMER2_CH1, TLI_B5, I2C0_SMBA, SPI0_MOSI, I2S0_SD, I2C3_SMBA, SPI2_MOSI, I2S2_SD, SPI5_MOSI, I2S5_SD, CAN1_RX, USBHS0_ULPI_D7, ETH0_PPS_OUT, EXMC_SDCKE1, DCI_D10, UART4_RX, EVENTOUT
PB6	92	I/O		Default: PB6 Alternate: TIMER15_MCH0, TIMER3_CH0, EXMC_D11, I2C0_SCL, I2C3_SCL, USART0_TX, CAN1_TX, OSPIM_P0_CSN, HPDF_DATAIN5, EXMC_SDNE1, DCI_D5, UART4_TX, EVENTOUT
PB7	93	I/O		Default: PB7 Alternate: TIMER16_MCH0, TIMER3_CH1, I2C0_SDA, I2C3_SDA, USART0_RX, HPDF_CKIN5, EXMC_NL, EXMC_NADV, DCI_VSYNC, EVENTOUT Additional: PVD_IN
BOOT	94	I/O		Default: BOOT
PB8	95	I/O		Default: PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, I2C3_SCL, SDIO0_CKIN, UART3_RX, CAN0_RX, SDIO1_D4, SDIO0_D4, DCI_D6, TLI_B6, EVENTOUT
PB9	96	I/O		Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, SPI1_NSS, I2S1_WS, I2C3_SDA,

LQFP100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				SDIO0_CMDDIR, UART3_TX, CAN0_TX, SDIO1_D5, I2C3_SMBA, SDIO0_D5, DCI_D7, TLI_B7, EVENTOUT
PE0	97	I/O		Default: PE0 Alternate: TIMER3_ETI, UART7_RX, SAI1_MCLK0, EXMC_NBL0, DCI_D2, TLI_R0, EVENTOUT
PE1	98	I/O		Default: PE1 Alternate: UART7_TX, EXMC_NBL1, DCI_D3, TLI_R6, EVENTOUT
VSS	99	P	-	Default: VSS
VDD	100	P	-	Default: VDD

(1) Type: I = input, O = output, P = power.
(2) I/O Level: 5VT = 5 V tolerant.
(3) USBHS0_DM and USBHS0_DP pins can only be used for USBHS.
(4) PC2_C and PC3_C can only be used as analog pins.

2.6.3. GD32H757Vx BGA100 pin definitions

Table 2-5. GD32H757Vx BGA100 pin definitions

BGA100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PE2	A3	I/O		Default: PE2 Alternate: TRACECK, SAI0_CLK0, SPI3_SCK, SAI0_MCLK0, OSPIM_P0_IO2, EXMC_A23, EVENTOUT
PE3	B3	I/O		Default: PE3 Alternate: TRACED0, TIMER14_BRKIN0, SAI0_SD1, EXMC_A19, DCI_PIXCLK, EVENTOUT
PE4	C3	I/O		Default: PE4 Alternate: TRACED1, TIMER0_BRKIN1, SAI0_DAT1, HPDF_DATAIN3, TIMER14_MCH0, SPI3_NSS, SAI0_FS0, EXMC_A20, DCI_D4, TLI_B0, EVENTOUT
PE5	D3	I/O		Default: PE5 Alternate: TRACED2, SAI0_CLK1, HPDF_CKIN3, TIMER14_CH0 , SPI3_MISO, SAI0_SCK0, EXMC_A21, DCI_D6, TLI_G0, EVENTOUT
PE6	E3	I/O		Default: PE6 Alternate: TRACED3, TIMER0_BRKIN2, SAI0_DAT0, TIMER14_CH1 , SPI3_MOSI, SAI0_SD0 , SAI1_MCLK1, CMP_MUX_OUT3, EXMC_A22, DCI_D7, TLI_G1, EVENTOUT
VSS	C2	P	-	Default: VSS
VDD	D2	P	-	Default: VDD

BGA100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
VBAT	B2	P	-	Default: VBAT
PC13	A2	I/O		Default: PC13 Alternate: EVENTOUT Additional: RTC_TAMP0, RTC_TS, WKUP3, RTC_OUT
PC14-OSC32IN	A1	I/O		Default: PC14 Alternate: EVENTOUT Additional: OSC32IN
PC15-OSC32OUT	B1	I/O		Default: PC15 Alternate: EVENTOUT Additional: OSC32OUT
PH0-OSCIN	C1	I/O		Default: PH0 Alternate: EVENTOUT Additional: OSCIN
PH1-OSCOUT	D1	I/O		Default: PH1 Alternate: EVENTOUT Additional: OSCOUT
NRST	E1	-	-	Default: NRST
PC0	F1	I/O		Default: PC0 Alternate: EXMC_D12, HPDF_CKIN0, HPDF_DATAIN4, TIMER40_CH0, SAI1_FS1, EXMC_A25, USBHS0_ULPI_STP, TLI_G2, EXMC_SDNWE, TRIGSEL_IN8, TLI_R5, EVENTOUT Additional: ADC012_IN10
PC1	F2	I/O		Default: PC1 Alternate: TRACED0, SAI0_DAT0, HPDF_DATAIN0, HPDF_CKIN4, SPI1_MOSI, I2S1_SD, SAI0_SD0, TIMER40_MCH0, SDIO1_CK, OSPIM_P0_IO4, ETH0_MDC, MDC, TRIGSEL_IN9, TLI_G5, EVENTOUT Additional: ADC012_IN11, RTC_TAMP2, WKUP5
PC2_C	E2	I/O		Default: PC2_C(4) Additional: ADC2_IN0
PC3_C	F3	I/O		Default: PC3_C(4) Additional: ADC2_IN1
VDD	K1	P	-	Default: VDD
VSS	J1	P	-	Default: VSS
VSSA	G1	P	-	Default: VSSA
VDDA	H1	P	-	Default: VDDA
PA0	G2	I/O		Default: PA0 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI, TIMER14_BRKIN0, SPI5_NSS, I2S5_WS, OSPIM_P0_IO6, USART1_CTS, UART3_TX, SDIO1_CMD, SAI1_SD1, EXMC_A19, TRIGSEL_IN0, EVENTOUT Additional: ADC0_IN16, WKUP0
PA1	H2	I/O		Default: PA1

BGA100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: TIMER1_CH1, TIMER4_CH1, TIMER14_MCH0, USART1_RTS, USART1_DE, UART3_RX, OSPIM_P0_IO3, SAI1_MCLK1, ETH0_RMII_REF_CLK, TRIGSEL_IN1, TLI_R2, EVENTOUT Additional: ADC0_IN17
PA2	J2	I/O		Default: PA2 Alternate: TIMER1_CH2, TIMER4_CH2, TIMER14_CH0, OSPIM_P0_IO0, USART1_TX, SAI1_SCK1, ETH0_MDIO, MDIO, TRIGSEL_IN7 , TLI_R1, EVENTOUT Additional: ADC01_IN14, WKUP1
PA3	K2	I/O		Default: PA3 Alternate: TIMER1_CH3, TIMER4_CH3, TIMER14_CH1, I2S5_MCK, OSPIM_P0_IO2, USART1_RX, TLI_B2, USBHS0_ULPI_D0, OSPIM_P0_SCK, TRIGSEL_IN4, TLI_B5, EVENTOUT Additional: ADC01_IN15
VDD	F4	P	-	Default: VDD
PA4	G3	I/O		Default: PA4 Alternate: TIMER4_ETI, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, USART1_CK, SPI5_NSS, I2S5_WS, EXMC_D8, DCI_HSYNC, TLI_VSYNC, EVENTOUT Additional: ADC01_IN18, DAC0_OUT0
PA5	H3	I/O		Default: PA5 Alternate: TIMER1_CH0, TIMER1_ETI, TIMER7_MCH0, SPI0_SCK, I2S0_CK, SPI5_SCK, I2S5_CK, USBHS0_ULPI_CK, MDIO_A0, EXMC_D9, TLI_R4, EVENTOUT Additional: ADC01_IN19, DAC0_OUT1
PA6	J3	I/O		Default: PA6 Alternate: TIMER0_BRKIN0, TIMER2_CH0, TIMER7_BRKIN0, SPI0_MISO, OSPIM_P0_IO3, SPI5_MISO, CMP_MUX_OUT0, MDIO_MDC, DCI_PIXCLK, TLI_G2, EVENTOUT Additional: ADC01_IN3
PA7	K3	I/O		Default: PA7 Alternate: TIMER0_MCH0, TIMER2_CH1, TIMER7_MCH0, SPI0_MOSI, I2S0_SD, SPI5_MOSI, I2S5_SD, OSPIM_P0_IO2, ETH0_RMII_CRS_DV, EXMC_SDNWE, TRIGSEL_IN5, TLI_VSYNC, EVENTOUT Additional: ADC01_IN7
PC4	G4	I/O		Default: PC4 Alternate: PMU_DEEPSLEEP, EXMC_A22, HPDF_CKIN2, I2S0_MCK, TIMER41_CH0, RSPDIF_CH2, SDIO1_CKIN, ETH0_RMII_RXD0, EXMC_SDNE0, TLI_R7, EVENTOUT

BGA100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Additional: ADC01_IN4, CMP0_IM7
PC5	H4	I/O		Default: PC5 Alternate: PMU_SLEEP, SAI0_DAT2, HPDF_DATAIN2, TIMER41_MCH0, RSPDIF_CH3, ETH0_RMII_RXD1, EXMC_SDCKE0, CMP0_OUT, TLI_DE, EVENTOUT Additional: ADC01_IN8
PB0	J4	I/O		Default: PB0 Alternate: TIMER0_MCH1, TIMER2_CH2, TIMER7_MCH1, OSPIM_P0_IO1, HPDF_CKOUT, UART3_CTS, TLI_R3, USBHS0_ULPI_D1, MDIO_A1, TRIGSEL_OUT3, TLI_G1, EVENTOUT Additional: ADC01_IN9, CMP0_IP0
PB1	K4	I/O		Default: PB1 Alternate: TIMER0_MCH2, TIMER2_CH3, TIMER7_MCH2, OSPIM_P0_IO0, HPDF_DATAIN1, TLI_R6, USBHS0_ULPI_D2, MDIO_A2, TRIGSEL_OUT4, TLI_G0, EVENTOUT Additional: ADC01_IN5, CMP0_IM6
PB2	G5	I/O		Default: PB2 Alternate: RTC_OUT, SAI0_DAT0, EXMC_D10, HPDF_CKIN1, SAI0_SD0, SPI2_MOSI, I2S2_SD, OSPIM_P0_SCK, EXMC_NCE, MDIO_A3, TIMER22_ETI, EVENTOUT Additional: CMP0_IP1
VDD	F5	P	-	Default: VDD
PE7	H5	I/O		Default: PE7 Alternate: TIMER0_ETI, HPDF_DATAIN2, UART6_RX, OSPIM_P0_IO4, EXMC_D4, EVENTOUT Additional: CMP1_IM7
PE8	J5	I/O		Default: PE8 Alternate: TIMER0_MCH0, HPDF_CKIN2, UART6_TX, OSPIM_P0_IO5, EXMC_D5, CMP1_OUT, EVENTOUT
PE9	K5	I/O		Default: PE9 Alternate: TIMER0_CH0, HPDF_CKOUT, SPI3_IO2, UART6_RTS, UART6_DE, OSPIM_P0_IO6, EXMC_D6, EVENTOUT Additional: CMP1_IP0
PE10	G6	I/O		Default: PE10 Alternate: TIMER0_MCH1, HPDF_DATAIN4, SPI3_IO3, UART6_CTS, OSPIM_P0_IO7, EXMC_D7, EVENTOUT Additional: CMP1_IM6
PE11	H6	I/O		Default: PE11 Alternate: TIMER0_CH1, HPDF_CKIN4, SPI3_NSS, SAI1_SD1, OSPIM_P0_CSN, EXMC_D8, TLI_G3, EVENTOUT

BGA100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Additional: CMP1_IP1
PE12	J6	I/O		Default: PE12 Alternate: TIMER0_MCH2, HPDF_DATAIN5, SPI3_SCK, SAI1_SCK1, EXMC_D9, CMP0_OUT, TLI_B4, EVENTOUT
PE13	K6	I/O		Default: PE13 Alternate: TIMER0_CH2, HPDF_CKIN5, SPI3_MISO, SAI1_FS1, EXMC_D10, CMP1_OUT, TLI_DE, EVENTOUT
PE14	G7	I/O		Default: PE14 Alternate: TIMER0_CH3, SPI3_MOSI, SAI1_MCLK1, EXMC_D11, TLI_PIXCLK, EVENTOUT
PE15	H7	I/O		Default: PE15 Alternate: TIMER0_BRKIN0, TLI_HSYNC, EXMC_D12, CMP_MUX_OUT4, TLI_R7, EVENTOUT
PB10	J7	I/O		Default: PB10 Alternate: TIMER1_CH2, I2C1_SCL, SPI1_SCK, I2S1_CK, HPDF_DATAIN7, USART2_TX, OSPIM_P0_CSN, USBHS0_ULPI_D3, TRIGSEL_OUT2, TLI_G4, EVENTOUT
PB11	K7	I/O		Default: PB11 Alternate: TIMER1_CH3, I2C1_SDA, HPDF_CKIN7, USART2_RX, USBHS0_ULPI_D4, ETH0_RMII_TX_EN, TLI_G5, EVENTOUT
VCORE	F8	P	-	Default: VCORE
PB12	K8	I/O	5VT	Default: PB12 Alternate: TIMER0_BRKIN0, I2C1_SMBA, SPI1_NSS, I2S1_WS, HPDF_DATAIN1, USART2_CK, CAN1_RX, USBHS0_ULPI_D5, ETH0_RMII_TXD0, OSPIM_P0_IO0, CMP_MUX_OUT2, UART4_RX, EVENTOUT
PB13	J8	I/O	5VT	Default: PB13 Alternate: RTC_REFIN, TIMER0_MCH0, OSPIM_P0_IO2, SPI1_SCK, I2S1_CK, HPDF_CKIN1, USART2_CTS, CAN1_TX, USBHS0_ULPI_D6, ETH0_RMII_TXD1, SDIO0_D0, DCI_D2, UART4_TX, EVENTOUT
PB14	H10	I/O		Default: PB14 Alternate: TIMER0_MCH1, TIMER7_MCH1, USART0_TX, SPI1_MISO, HPDF_DATAIN2, USART2_RTS, USART2_DE, UART3_RTS, UART3_DE, SDIO1_D0, EXMC_D10, TRIGSEL_OUT1, TLI_PIXCLK, EVENTOUT
PB15	G10	I/O		Default: PB15 Alternate: RTC_REFIN, TIMER0_MCH2, TIMER7_MCH2, USART0_RX, SPI1_MOSI, I2S1_SD, HPDF_CKIN2, UART3_CTS, SDIO1_D1, EXMC_D11, TRIGSEL_OUT5, TLI_G7, EVENTOUT
PD8	K9	I/O		Default: PD8 Alternate: HPDF_CKIN3, USART2_TX, SAI1_CLK0, RSPDIF_CH1, EXMC_D13, EVENTOUT

BGA100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
PD9	J9	I/O		Default: PD9 Alternate: HPDF_DATAIN3, USART2_RX, SAI1_CLK1, EXMC_D14, EVENTOUT
PD10	H9	I/O		Default: PD10 Alternate: HPDF_CKOUT, USART2_CK, SAI1_DAT1, EXMC_D15, TLI_B3, EVENTOUT
PD11	G9	I/O		Default: PD11 Alternate: TIMER40_CH1, TIMER7_MCH3, I2C3_SMBA, USART2_CTS, SAI1_DAT2, OSPIM_P0_IO0, SAI1_SD0, EXMC_A16, EXMC_CLE, EVENTOUT
PD12	K10	I/O		Default: PD12 Alternate: TIMER41_CH1, TIMER3_CH0, I2C3_SCL, CAN2_RX, EDOUT_A, USART2_RTS, USART2_DE, OSPIM_P0_IO1, SAI1_FS0, EXMC_A17, EXMC_ALE, DCI_D12, EVENTOUT
PD13	J10	I/O		Default: PD13 Alternate: TIMER42_CH1, TIMER3_CH1, I2C3_SDA, CAN2_TX, EDOUT_B, OSPIM_P0_IO3, SAI1_SCK0, EXMC_A18, DCI_D13, EVENTOUT
PD14	H8	I/O		Default: PD14 Alternate: TIMER43_CH1, TIMER3_CH2, SPI3_IO2, EDOUT_Z, UART7_CTS, EXMC_D0, EVENTOUT
PD15	G8	I/O		Default: PD15 Alternate: TIMER44_CH1, TIMER3_CH3, SPI3_IO3, UART7_RTS, UART7_DE, EXMC_D1, EVENTOUT
VDD33USB	F6	P	-	Default: VDD33USB
PC6	F10	I/O		Default: PC6 Alternate: TIMER0_BRKIN1, TIMER2_CH0, TIMER7_CH0, HPDF_CKIN3, I2S1_MCK, USART5_TX, SDIO0_DAT0DIR, EXMC_NWAIT, SDIO1_D6, SDIO0_D6, DCI_D0, TLI_HSYNC, EVENTOUT
PC7	E10	I/O		Default: PC7 Alternate: TIMER0_CH3, TIMER2_CH1, TIMER7_CH1, HPDF_DATAIN3, I2S2_MCK, USART5_RX, SDIO0_DAT123DIR, EXMC_NE0, SDIO1_D7, SDIO0_D7, DCI_D1, TLI_G6, EVENTOUT
PC8	F9	I/O		Default: PC8 Alternate: TRACED1, TIMER2_CH2, TIMER7_CH2, USART5_CK, UART4_RTS, UART4_DE, EXMC_NE1, EXMC_INT, SDIO0_D0, DCI_D2, EVENTOUT
PC9	E9	I/O		Default: PC9 Alternate: CK_OUT1, TIMER0_MCH3, TIMER2_CH3, TIMER7_CH3, I2C2_SDA, I2S_CKIN, UART4_CTS, OSPIM_P0_IO0, TLI_G3, SDIO0_D1, DCI_D3, TLI_B2,

BGA100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				EVENTOUT
PA8	D9	I/O		Default: PA8 Alternate: CK_OUT0, TIMER0_CH0, TIMER7_BRKIN2, I2C2_SCL, USART0_CK, USBHS0_SOF, UART6_RX, CMP_MUX_OUT1, TLI_B3, TLI_R6, EVENTOUT
PA9	C9	I/O	5VT	Default: PA9 Alternate: TIMER0_CH1, I2C2_SMBA, SPI1_SCK, I2S1_CK, USART0_TX, TRIGSEL_IN13, DCI_D0, TLI_R5, EVENTOUT Additional: USBHS0_VBUS
PA10	D10	I/O	5VT	Default: PA10 Alternate: TIMER0_CH2, USART0_RX, TRIGSEL_IN12, USBHS0_ID, MDIO, TLI_B4, DCI_D1, TLI_B1, EVENTOUT
USBHS0_DM	C10	I/O		Default: USBHS0_DM(3)
USBHS0_DP	B10	I/O		Default: USBHS0_DP(3)
PA13	A10	I/O		Default: JTMS, SWDIO, PA13 Alternate: TIMER0_BRKIN1, TIMER7_BRKIN1, SPI1_NSS, I2S1_WS, UART3_RX, USART0_CTS, CAN0_RX, MDIO_A3, EXMC_INT, TRIGSEL_IN10, TLI_R4, EVENTOUT
VCORE	E7	P	-	Default: VCORE
VSS	E5	P	-	Default: VSS
PA14	A9	I/O		Default: JTCK, SWCLK, PA14 Alternate: TLI_G7, SPI1_SCK, I2S1_CK, UART3_TX, USART0_RTS, USART0_DE, SAI1_FS1, CAN0_TX, MDIO_A4, TIMER0_BRKIN2, TRIGSEL_IN11, TLI_R5, EVENTOUT
PA15	A8	I/O		Default: JTDI, PA15 Alternate: TIMER1_CH0, TIMER1_ETI, SPI0_NSS, I2S0_WS, SPI2_NSS, I2S2_WS, SPI5_NSS, I2S5_WS, UART3_RTS, UART3_DE, TLI_R3, UART6_TX, MDIO_A0, TRIGSEL_OUT0, TLI_B6, EVENTOUT
PC10	B9	I/O		Default: PC10 Alternate: TIMER0_CH3, HPDF_CKIN5, SPI2_SCK, I2S2_CK, USART2_TX, UART3_TX, OSPIM_P0_IO1, TLI_B1, MDIO_A1, SDIO0_D2, DCI_D8, TLI_R2, EVENTOUT
PC11	B8	I/O		Default: PC11 Alternate: TIMER0_ETI, HPDF_DATAIN5, SPI2_MISO, USART2_RX, UART3_RX, OSPIM_P0_CSN, EXMC_NBL2, MDIO_A2, SDIO0_D3, DCI_D4, TLI_B4, EVENTOUT
PC12	C8	I/O		Default: PC12

BGA100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				Alternate: TRACED3, EXMC_D6, TIMER14_CH0, SPI5_SCK, I2S5_CK, SPI2_MOSI, I2S2_SD, USART2_CK, UART4_TX, SDIO0_CK, DCI_D9, TLI_R6, EVENTOUT
PD0	D8	I/O		Default: PD0 Alternate: TIMER7_CH2, HPDF_CKIN6, UART3_RX, CAN0_RX, EXMC_D2, TRIGSEL_IN3, TLI_B1, EVENTOUT
PD1	E8	I/O		Default: PD1 Alternate: HPDF_DATAIN6, UART3_TX, CAN0_TX, EXMC_D3, TRIGSEL_IN6, EVENTOUT
PD2	B7	I/O		Default: PD2 Alternate: TRACED2, EXMC_D7, TIMER2_ETI, TIMER14_BRKIN0, UART4_RX, TLI_B7, SDIO0_CMD, DCI_D11, TLI_B2, EVENTOUT
PD3	C7	I/O		Default: PD3 Alternate: HPDF_CKOUT, SPI1_SCK, I2S1_CK, USART1_CTS, EXMC_CLK, DCI_D5, TLI_G7, EVENTOUT
PD4	D7	I/O		Default: PD4 Alternate: TIMER7_MCH3, USART1_RTS, USART1_DE, OSPIM_P0_IO4, EXMC_NOE, EVENTOUT
PD5	B6	I/O		Default: PD5 Alternate: TIMER7_CH3, USART1_TX, OSPIM_P0_IO5, EXMC_NWE, EVENTOUT
PD6	C6	I/O		Default: PD6 Alternate: SAI1_DAT0, SAI0_DAT0, HPDF_CKIN4, HPDF_DATAIN1, SPI2_MOSI, I2S2_SD, SAI0_SD0, USART1_RX, OSPIM_P0_IO6, SDIO1_CK, EXMC_NWAIT, DCI_D10, TLI_B2, EVENTOUT
PD7	D6	I/O		Default: PD7 Alternate: HPDF_DATAIN4, SPI0_MOSI, I2S0_SD, HPDF_CKIN1, USART1_CK, RSPDIF_CH0, OSPIM_P0_IO7, SDIO1_CMD, EXMC_NE0, EXMC_NCE, EVENTOUT
VSS	E6	P	-	Default: VSS
PB3	A7	I/O		Default: JTDO, PB3 Alternate: TRACESWO, TIMER1_CH1, TLI_PIXCLK, SPI0_SCK, I2S0_CK, SPI2_SCK, I2S2_CK, SPI5_SCK, I2S5_CK, SDIO1_D2, CTC_SYNC, UART6_RX, MDIO_A4, TRIGSEL_OUT7, TIMER23_ETI, EVENTOUT
PB4	A6	I/O		Default: NJTRST, PB4 Alternate: TIMER15_BRKIN0, TIMER2_CH0, SPI0_MISO, SPI2_MISO, SPI1_NSS, I2S1_WS, SPI5_MISO, SDIO1_D3, UART6_TX, TRIGSEL_OUT6, EVENTOUT
PB5	C5	I/O		Default: PB5 Alternate: TIMER16_BRKIN0, TIMER2_CH1, TLI_B5,

BGA100				
Pin Name	Pins	Pin Type(1)	I/O Level(2)	Functions description
				I2C0_SMBA, SPI0_MOSI, I2S0_SD, I2C3_SMBA, SPI2_MOSI, I2S2_SD, SPI5_MOSI, I2S5_SD, CAN1_RX, USBHS0_ULPI_D7, ETH0_PPS_OUT, EXMC_SDCKE1, DCI_D10, UART4_RX, EVENTOUT
PB6	B5	I/O		Default: PB6 Alternate: TIMER15_MCH0, TIMER3_CH0, EXMC_D11, I2C0_SCL, I2C3_SCL, USART0_TX, CAN1_TX, OSPIM_P0_CSN, HPDF_DATAIN5, EXMC_SDNE1, DCI_D5, UART4_TX, EVENTOUT
PB7	A5	I/O		Default: PB7 Alternate: TIMER16_MCH0, TIMER3_CH1, I2C0_SDA, I2C3_SDA, USART0_RX, HPDF_CKIN5, EXMC_NL, EXMC_NADV, DCI_VSYNC, EVENTOUT Additional: PVD_IN
BOOT	D5	I/O		Default: BOOT
PB8	B4	I/O		Default: PB8 Alternate: TIMER15_CH0, TIMER3_CH2, HPDF_CKIN7, I2C0_SCL, I2C3_SCL, SDIO0_CKIN, UART3_RX, CAN0_RX, SDIO1_D4, SDIO0_D4, DCI_D6, TLI_B6, EVENTOUT
PB9	A4	I/O		Default: PB9 Alternate: TIMER16_CH0, TIMER3_CH3, HPDF_DATAIN7, I2C0_SDA, SPI1_NSS, I2S1_WS, I2C3_SDA, SDIO0_CMDDIR, UART3_TX, CAN0_TX, SDIO1_D5, I2C3_SMBA, SDIO0_D5, DCI_D7, TLI_B7, EVENTOUT
PE0	D4	I/O		Default: PE0 Alternate: TIMER3_ETI, UART7_RX, SAI1_MCLK0, EXMC_NBL0, DCI_D2, TLI_R0, EVENTOUT
PE1	C4	I/O		Default: PE1 Alternate: UART7_TX, EXMC_NBL1, DCI_D3, TLI_R6, EVENTOUT
VSS	E4	P	-	Default: VSS
PDR_ON	F7	P	-	Default: PDR_ON(5)

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) USBHS0_DM and USBH0_DP pins can only be used for USBHS.

(4) PC2_C and PC3_C can only be used as analog pins.

(5) PDR_ON pin should be pulled up to V_{DD}, refer to ***Figure 4-2. Recommended PDR_ON pin circuit(1)***.

2.6.4. GD32H757xx pin alternate functions

Table 2-6. Port A alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA0		TIMER1_CH0/TIMER1_ETI	TIMER4_CH0	TIMER7_ETI	TIMER14_BRKIN0	SPI5_NSS/I2S5_WS	OSPIM_P0_IO6	USART1_CTS	UART3_TX	SDIO1_CMD	SAI1_SD1		EXMC_A19	TRIGSEL_IN0		EVENTOUT
PA1		TIMER1_CH1	TIMER4_CH1		TIMER14_MCH0			USART1_RTS/USART1_DE	UART3_RX	OSPIM_P0_IO3	SAI1_MCLK1	ETH0_RMII_REF_CLK		TRIGSEL_IN1	TLI_R2	EVENTOUT
PA2		TIMER1_CH2	TIMER4_CH2		TIMER14_CH0		OSPIM_P0_IO0	USART1_TX	SAI1_SCK1			ETH0_MDIO	MDIO	TRIGSEL_IN7	TLI_R1	EVENTOUT
PA3		TIMER1_CH3	TIMER4_CH3		TIMER14_CH1	I2S5_MCK	OSPIM_P0_IO2	USART1_RX		TLI_B2	USBHS0_ULPI_D0		OSPIM_P0_SCK	TRIGSEL_IN4	TLI_B5	EVENTOUT
PA4			TIMER4_ETI			SPI0_NSS/I2S0_WS	SPI2_NSS/I2S2_WS	USART1_CK	SPI5_NSS/I2S5_WS				EXMC_D8	DCI_HSYNC	TLI_VSYNC	EVENTOUT
PA5		TIMER1_CH0/TIMER1_ETI		TIMER7_MCH0		SPI0_SCK/I2S0_CK			SPI5_SCK/I2S5_CK		USBHS0_ULPI_CK	MDIO_A0	EXMC_D9		TLI_R4	EVENTOUT
PA6		TIMER0_BRKIN0	TIMER2_CH0	TIMER7_BRKIN0		SPI0_MISO	OSPIM_P0_IO3		SPI5_MISO		CMP_MUX_OUT0	MDIO_MDC		DCI_PIXCLK	TLI_G2	EVENTOUT
PA7		TIMER0_MCH0	TIMER2_CH1	TIMER7_MCH0		SPI0_MOSI/I2S0_SD			SPI5_MOSI/I2S5_SD		OSPIM_P0_IO2	ETH0_RMII_CRS_DV	EXMC_SDNWE	TRIGSEL_IN5	TLI_VSYNC	EVENTOUT
PA8	CK_OUT0	TIMER0_CH0		TIMER7_BRKIN2	I2C2_SCL			USART0_CK			USBHS0_SOF	UART6_RX	CMP_MUX_OUT1	TLI_B3	TLI_R6	EVENTOUT
PA9		TIMER0_CH1			I2C2_SMBA	SPI1_SCK/I2S1_CK		USART0_TX		TRIGSEL_IN13				DCI_D0	TLI_R5	EVENTOUT
PA10		TIMER0_CH2						USART0_RX			USBHS0_ID	MDIO	TLI_B4	DCI_D1	TLI_B1	EVENTOUT
PA13	JTMS/SWDIO	TIMER0_BRKIN1		TIMER7_BRKIN1		SPI1_NSS/I2S1_WS	UART3_RX	USART0_CTS		CAN0_RX		MDIO_A3	EXMC_INT	TRIGSEL_IN10	TLI_R4	EVENTOUT
PA14	JTCK/SWCLK				TLI_G7	SPI1_SCK/I2S1_CK	UART3_TX	USART0_RTS/USART0_DE	SAI1_FS1	CAN0_TX		MDIO_A4	TIMER0_BRKIN2	TRIGSEL_IN11	TLI_R5	EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PA15	JTDI	TIMER1_CH0/TIMER1_ETI				SPI0_NSS/I2S0_WS	SPI2_NSS/I2S2_WS	SPI5_NSS/I2S5_WS	UART3_RTS/UART3_DE	TLI_R3		UART6_TX	MDIO_A0	TRIGSEL_OUT0	TLI_B6	EVENTOUT

Table 2-7. Port B alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB0		TIMER0_MCH1	TIMER2_CH2	TIMER7_MCH1	OSPIM_P0_IO1		HPDF_CKOUT		UART3_CTS	TLI_R3	USBHS0_ULPI_D1		MDIO_A1	TRIGSEL_OUT3	TLI_G1	EVENTOUT
PB1		TIMER0_MCH2	TIMER2_CH3	TIMER7_MCH2	OSPIM_P0_IO0		HPDF_DATAIN1			TLI_R6	USBHS0_ULPI_D2		MDIO_A2	TRIGSEL_OUT4	TLI_G0	EVENTOUT
PB2	RTC_OUT	SAI2_DAT0[1]	SAI0_DAT0	EXMC_D10	HPDF_CKIN1		SAI0_SD0	SPI2_MOSI/I2S2_SD	SAI2_SD0[1]	OSPIM_P0_SCK		EXMC_NCE	MDIO_A3	TIMER22_ETI		EVENTOUT
PB3	JTDO/TRACESWO	TIMER1_CH1	TLI_PIXCLK			SPI0_SCK/I2S0_CK	SPI2_SCK/I2S2_CK		SPI5_SCK/I2S5_CK	SDIO1_D2	CTC_SYNC	UART6_RX	MDIO_A4	TRIGSEL_OUT7	TIMER23_ETI	EVENTOUT
PB4	NJTRST	TIMER15_BRKIN0	TIMER2_CH0			SPI0_MISO	SPI2_MISO	SPI1_NSS/I2S1_WS	SPI5_MISO	SDIO1_D3		UART6_TX		TRIGSEL_OUT6		EVENTOUT
PB5		TIMER16_BRKIN0	TIMER2_CH1	TLI_B5	I2C0_SMBA	SPI0_MOSI/ I2S0_SD	I2C3_SMBA	SPI2_MOSI/I2S2_SD	SPI5_MOSI/I2S5_SD	CAN1_RX	USBHS0_ULPI_D7	ETH0_PPS_OUT	EXMC_SDCKE1	DCI_D10	UART4_RX	EVENTOUT
PB6		TIMER15_MCH0	TIMER3_CH0	EXMC_D11	I2C0_SCL		I2C3_SCL	USART0_TX		CAN1_TX	OSPIM_P0_CSN	HPDF_DATAIN5	EXMC_SDNE1	DCI_D5	UART4_TX	EVENTOUT
PB7		TIMER16_MCH0	TIMER3_CH1		I2C0_SDA		I2C3_SDA	USART0_RX				HPDF_CKIN5	EXMC_NL/EXMC_NADV,	DCI_VSYNC		EVENTOUT
PB8		TIMER15_CH0	TIMER3_CH2	HPDF_CKIN7	I2C0_SCL		I2C3_SCL	SDIO0_CKIN	UART3_RX	CAN0_RX	SDIO1_D4		SDIO0_D4	DCI_D6	TLI_B6	EVENTOUT
PB9		TIMER16_CH0	TIMER3_CH3	HPDF_DATAIN7	I2C0_SDA	SPI1_NSS/I2S1_WS	I2C3_SDA	SDIO0_CMDDIR	UART3_TX	CAN0_TX	SDIO1_D5	I2C3_SMBA	SDIO0_D5	DCI_D7	TLI_B7	EVENTOUT
PB10		TIMER1_CH2			I2C1_SCL	SPI1_SCK/I2S1_CK	HPDF_DATAIN7	USART2_TX		OSPIM_P0_CSN	USBHS0_ULPI_D3			TRIGSEL_OUT2	TLI_G4	EVENTOUT
PB11		TIMER1_CH3			I2C1_SDA		HPDF_CKIN7	USART2_RX			USBHS0_ULPI_D4	ETH0_RMII_TX_EN			TLI_G5	EVENTOUT
PB12		TIMER0_BRKIN0			I2C1_SMBA	SPI1_NSS/I2S1_WS	HPDF_DATAIN1	USART2_CK		CAN1_RX	USBHS0_ULPI_D5	ETH0_RMII_TXD0	OSPIM_P0_IO0	CMP_MUX_OUT2	UART4_RX	EVENTOUT
PB13	RTC_REFIN	TIMER0_MCH0			OSPIM_P0_IO2	SPI1_SCK/I2S1_CK	HPDF_CKIN1	USART2_CTS		CAN1_TX	USBHS0_ULPI_D6	ETH0_RMII_TXD1	SDIO0_D0	DCI_D2	UART4_TX	EVENTOUT
PB14		TIMER0_MCH1		TIMER7_MCH1	USART0_TX	SPI1_MISO	HPDF_DATAIN2	USART2_RTS/USART2_DE	UART3_RTS/UART3_DE	SDIO1_D0			EXMC_D10	TRIGSEL_OUT1	TLI_CLK	EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PB15	RTC_REFIN	TIMER0_MCH2		TIMER7_MCH2	USART0_RX	SPI1_MOSI/I2S1_SD	HPDF_CKIN2		UART3_CTS	SDIO1_D1			EXMC_D11	TRIGSEL_OUT5	TLI_G7	EVENTOUT

Table 2-8. Port C alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PC0		EXMC_D12		HPDF_CKIN0			HPDF_DATAIN4	TIMER40_CH0	SAI1_FS1	EXMC_A25	USBHS0_ULPI_STP	TLI_G2	EXMC_SDNWE	TRIGSEL_IN8	TLI_R5	EVENTOUT
PC1	TRACED0	SAI2_DAT0(1)	SAI0_DAT0	HPDF_DATAIN0	HPDF_CKIN4	SPI1_MOSI/I2S1_SD	SAI0_SD0	TIMER40_MCH0	SAI2_SD0(1)	SDIO1_CK	OSPIM_P0_IO4	ETH0_MDC	MDC	TRIGSEL_IN9	TLI_G5	EVENTOUT
PC4	PMU_DEEPSLEEP	EXMC_A22		HPDF_CKIN2		I2S0_MCK		TIMER41_CH0		RSPDIF_CH2	SDIO1_CKIN	ETH0_RMII_RXD0	EXMC_SDNE0		TLI_R7	EVENTOUT
PC5	PMU_SLEEP	SAI2_DAT2(1)	SAI0_DAT2	HPDF_DATAIN2				TIMER41_MCH0		RSPDIF_CH3		ETH0_RMII_RXD1	EXMC_SDCKE0	CMP0_OUT	TLI_DE	EVENTOUT
PC6		TIMER0_BRKIN1	TIMER2_CH0	TIMER7_CH0	HPDF_CKIN3	I2S1_MCK		USART5_TX	SDIO0_DAT0DIR	EXMC_NWAIT	SDIO1_D6		SDIO0_D6	DCI_D0	TLI_HSYNC	EVENTOUT
PC7		TIMER0_CH3	TIMER2_CH1	TIMER7_CH1	HPDF_DATAIN3		I2S2_MCK	USART5_RX	SDIO0_DAT123DIR	EXMC_NE0	SDIO1_D7		SDIO0_D7	DCI_D1	TLI_G6	EVENTOUT
PC8	TRACED1		TIMER2_CH2	TIMER7_CH2				USART5_CK	UART4_RTS/UART4_DE	EXMC_NE1	EXMC_INT		SDIO0_D0	DCI_D2		EVENTOUT
PC9	CK_OUT1	TIMER0_MCH3	TIMER2_CH3	TIMER7_CH3	I2C2_SDA	I2S_CKIN			UART4_CTS	OSPIM_P0_IO0	TLI_G3		SDIO0_D1	DCI_D3	TLI_B2	EVENTOUT
PC10		TIMER0_CH3		HPDF_CKIN5			SPI2_SCK/I2S2_CK	USART2_TX	UART3_TX	OSPIM_P0_IO1	TLI_B1	MDIO_A1	SDIO0_D2	DCI_D8	TLI_R2	EVENTOUT
PC11		TIMER0_ETI		HPDF_DATAIN5			SPI2_MISO	USART2_RX	UART3_RX	OSPIM_P0_CSN	EXMC_NBL2	MDIO_A2	SDIO0_D3	DCI_D4	TLI_B4	EVENTOUT
PC12	TRACED3	EXMC_D6	TIMER14_CH0			SPI5_SCK/I2S5_CK	SPI2_MOSI/I2S2_SD	USART2_CK	UART4_TX				SDIO0_CK	DCI_D9	TLI_R6	EVENTOUT
PC13																EVENTOUT
PC14																EVENTOUT
PC15																EVENTOUT

Table 2-9. Port D alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PD0			TIMER7_CH2	HPDF_CKIN6					UART3_RX	CAN0_RX			EXMC_D2	TRIGSEL_IN3	TLI_B1	EVENTOUT
PD1				HPDF_DATAIN6					UART3_TX	CAN0_TX			EXMC_D3	TRIGSEL_IN6		EVENTOUT
PD2	TRACED2	EXMC_D7	TIMER2_ETI		TIMER14_BRKIN0				UART4_RX	TLI_B7			SDIO0_CMD	DCI_D11	TLI_B2	EVENTOUT
PD3				HPDF_CKOUT		SPI1_SCK/I2S1_CK		USART1_CTS					EXMC_CLK	DCI_D5	TLI_G7	EVENTOUT
PD4				TIMER7_MCH3				USART1_RTS/USART1_DE			OSPIM_P0_IO4		EXMC_NOE			EVENTOUT
PD5				TIMER7_CH3				USART1_TX			OSPIM_P0_IO5		EXMC_NWE			EVENTOUT
PD6		SAI1_DAT0	SAI0_DAT0	HPDF_CKIN4	HPDF_DATAIN1	SPI2_MOSI/I2S2_SD	SAI0_SD0	USART1_RX	SAI2_SD0 (1)		OSPIM_P0_IO6	SDIO1_CK	EXMC_NWAIT	DCI_D10	TLI_B2	EVENTOUT
PD7				HPDF_DATAIN4		SPI0_MOSI/I2S0_SD	HPDF_CKIN1	USART1_CK		RSPDIF_CH0	OSPIM_P0_IO7	SDIO1_CMD	EXMC_NE0/EXMC_NCE			EVENTOUT
PD8				HPDF_CKIN3				USART2_TX	SAI1_CLK0	RSPDIF_CH1			EXMC_D13			EVENTOUT
PD9				HPDF_DATAIN3				USART2_RX	SAI1_CLK1				EXMC_D14			EVENTOUT
PD10				HPDF_CKOUT				USART2_CK	SAI1_DAT1				EXMC_D15		TLI_B3	EVENTOUT
PD11	TIMER40_CH1			TIMER7_MCH3	I2C3_SMBA			USART2_CTS	SAI1_DAT2	OSPIM_P0_IO0	SAI1_SD0		EXMC_A16/EXMC_CLE			EVENTOUT
PD12	TIMER41_CH1		TIMER3_CH0		I2C3_SCL	CAN2_RX	EDOUT_A	USART2_RTS/USART2_DE		OSPIM_P0_IO1	SAI1_FS0		EXMC_A17/EXMC_ALE	DCI_D12		EVENTOUT
PD13	TIMER42_CH1		TIMER3_CH1		I2C3_SDA	CAN2_TX	EDOUT_B			OSPIM_P0_IO3	SAI1_SCK0		EXMC_A18	DCI_D13		EVENTOUT
PD14	TIMER43_CH1		TIMER3_CH2			SPI3_IO2	EDOUT_Z		UART7_CTS				EXMC_D0			EVENTOUT
PD15	TIMER44_CH1		TIMER3_CH3			SPI3_IO3			UART7_RTS/UART7_DE				EXMC_D1			EVENTOUT

Table 2-10. Port E alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PE0			TIMER3_ETI						UART7_RX		SAI1_MCLK0		EXMC_NBL0	DCI_D2	TLI_R0	EVENTOUT
PE1									UART7_TX				EXMC_NBL1	DCI_D3	TLI_R6	EVENTOUT
PE2	TRACECK		SAI0_CLK0			SPI3_SCK	SAI0_MCLK0		SAI2_MCLK0(1)	OSPIM_P0_IO2	SAI2_CLK0(1)		EXMC_A23			EVENTOUT
PE3	TRACED0				TIMER14_BRKIN0		SAI0_SD1		SAI2_SD1(1)				EXMC_A19	DCI_PIXCLK		EVENTOUT
PE4	TRACED1	TIMER0_BRKIN1	SAI0_DAT1	HPDF_DATAIN3	TIMER14_MCH0	SPI3_NSS	SAI0_FS0		SAI2_FS0(1)		SAI2_DAT1(1)		EXMC_A20	DCI_D4	TLI_B0	EVENTOUT
PE5	TRACED2		SAI0_CLK1	HPDF_CKIN3	TIMER14_CH0	SPI3_MISO	SAI0_SCK0		SAI2_SCK0(1)		SAI2_CLK1(1)		EXMC_A21	DCI_D6	TLI_G0	EVENTOUT
PE6	TRACED3	TIMER0_BRKIN2	SAI0_DAT0		TIMER14_CH1	SPI3_MOSI	SAI0_SD0		SAI2_SD0(1)	SAI2_DAT0	SAI1_MCLK1	CMP_MUX_OUT3	EXMC_A22	DCI_D7	TLI_G1	EVENTOUT
PE7		TIMER0_ETI		HPDF_DATAIN2				UART6_RX			OSPIM_P0_IO4		EXMC_D4			EVENTOUT
PE8		TIMER0_MCH0		HPDF_CKIN2				UART6_TX			OSPIM_P0_IO5		EXMC_D5	CMP1_OUT		EVENTOUT
PE9		TIMER0_CH0		HPDF_CKOUT		SPI3_IO2		UART6_RTS/UART6_DE			OSPIM_P0_IO6		EXMC_D6			EVENTOUT
PE10		TIMER0_MCH1		HPDF_DATAIN4		SPI3_IO3		UART6_CTS			OSPIM_P0_IO7		EXMC_D7			EVENTOUT
PE11		TIMER0_CH1		HPDF_CKIN4		SPI3_NSS					SAI1_SD1	OSPIM_P0_CSN	EXMC_D8		TLI_G3	EVENTOUT
PE12		TIMER0_MCH2		HPDF_DATAIN5		SPI3_SCK					SAI1_SCK1		EXMC_D9	CMP0_OUT	TLI_B4	EVENTOUT
PE13		TIMER0_CH2		HPDF_CKIN5		SPI3_MISO					SAI1_FS1		EXMC_D10	CMP1_OUT	TLI_DE	EVENTOUT
PE14		TIMER0_CH3				SPI3_MOSI					SAI1_MCLK1		EXMC_D11		TLI_PIXCLK	EVENTOUT
PE15		TIMER0_BRKIN0									TLI_HSYNC		EXMC_D12	CMP_MUX_OUT4	TLI_R7	EVENTOUT

Table 2-11. Port F alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PF0					I2C1_SDA	USBHS0_ULPI_D4				OSPIM_P1_IO0			EXMC_A0	TIMER22_CH0		EVENTOUT
PF1					I2C1_SCL	USBHS0_ULPI_D5				OSPIM_P1_IO1			EXMC_A1	TIMER22_CH1		EVENTOUT
PF2					I2C1_SMBA	USBHS0_ULPI_D6				OSPIM_P1_IO2			EXMC_A2	TIMER22_CH2		EVENTOUT
PF3										OSPIM_P1_IO3			EXMC_A3	TIMER22_CH3		EVENTOUT
PF4		TIMER0_MCH1		TIMER7_MCH1	USART0_TX		HPDF_DATAIN2	USART2_RTS/USART2_DE	UART3_RTS/UART3_DE	OSPIM_P1_SCK	SDIO1_D0		EXMC_A4	TRIGSEL_OUT1	TLI_PIXCLK	EVENTOUT
PF5		TIMER0_MCH2,		TIMER7_MCH2	USART0_RX		HPDF_CKIN2		UART3_CTS		SDIO1_D1		EXMC_A5	TRIGSEL_OUT5	TLI_G7	EVENTOUT
PF6		TIMER15_CH0	CAN2_RX			SPI4_NSS	SAI0_SD1	UART6_RX	SAI2_SD1		OSPIM_P0_IO3		EXMC_D24	TIMER22_CH0		EVENTOUT
PF7		TIMER16_CH0	CAN2_TX			SPI4_SCK	SAI0_MCLK1	UART6_TX	SAI2_MCLK1		OSPIM_P0_IO2		EXMC_D25	TIMER22_CH1		EVENTOUT
PF8		TIMER15_MCH0				SPI4_MISO	SAI0_SCK1	UART6_RTS/UART6_DE	SAI2_SCK1		OSPIM_P0_IO0		EXMC_D26	TIMER22_CH2		EVENTOUT
PF9		TIMER16_MCH0				SPI4_MOSI	SAI0_FS1	UART6_CTS	SAI2_FS1		OSPIM_P0_IO1		EXMC_D27	TIMER22_CH3		EVENTOUT
PF10		TIMER15_BRKIN0	SAI0_DAT2							OSPIM_P0_SCK	SAI2_DAT2			DCI_D11	TLI_DE	EVENTOUT
PF11						SPI4_MOSI					SAI1_SD1		EXMC_SDNRAS	DCI_D12	TIMER23_CH0	EVENTOUT
PF12													EXMC_A6		TIMER23_CH1	EVENTOUT
PF13				HPDF_DATAIN6	I2C3_SMBA								EXMC_A7		TIMER23_CH2	EVENTOUT
PF14				HPDF_CKIN6	I2C3_SCL	SPI4_IO2							EXMC_A8		TIMER23_CH3	EVENTOUT
PF15					I2C3_SDA	SPI4_IO3							EXMC_A9			EVENTOUT

Table 2-12. Port G alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PG0					TIMER31_CH0					OSPIM_P1_IO4			EXMC_A10			EVENTOUT
PG1					TIMER31_CH1					OSPIM_P1_IO5			EXMC_A11			EVENTOUT
PG2		TIMER0_BRKIN1		TIMER7_BRKIN0	TIMER31_CH2	SPI1_MISO						CMP_MUX_OUT5	EXMC_A12		TIMER23_ETI	EVENTOUT
PG3				TIMER7_BRKIN2	TIMER31_CH3	SPI1_MOSI/I2S1_SD						CMP_MUX_OUT6	EXMC_A13	TIMER22_ETI		EVENTOUT
PG4		TIMER0_BRKIN2		TIMER7_BRKIN1	TIMER31_ETI							CMP_MUX_OUT7	EXMC_A14			EVENTOUT
PG5		TIMER0_ETI			TIMER30_CH0								EXMC_A15			EVENTOUT
PG6		TIMER16_BRKIN0			TIMER30_CH1						OSPIM_P0_CSN		EXMC_NE2	DCI_D12	TLI_R7	EVENTOUT
PG7		EXMC_D28			TIMER30_CH2		SAI0_MCLK0	USART5_CK					EXMC_INT	DCI_D13	TLI_PIXCLK	EVENTOUT
PG8				TIMER7_ETI	TIMER30_CH3	SPI5_NSS/I2S5_WS		USART5_RTS/USART5_DE	RSPDIF_CH2			ETH0_PPS_OUT	EXMC_SDCLK		TLI_G7	EVENTOUT
PG9		EXMC_D30	CAN2_TX	TIMER7_BRKIN1	TIMER30_ETI	SPI0_MISO		USART5_RX	RSPDIF_CH3	OSPIM_P0_IO6	SAI1_FS1	SDIO1_D0	EXMC_NE1	DCI_VSYNC		EVENTOUT
PG10		EXMC_D31	CAN2_RX	OSPIM_P1_IO6		SPI0_NSS/I2S0_WS				TLI_G3	SAI1_SD1	SDIO1_D1	EXMC_NE2	DCI_D2	TLI_B2	EVENTOUT
PG11			EXMC_D29			SPI0_SCK/I2S0_CK			RSPDIF_CH0	OSPIM_P1_IO7	SDIO1_D2	ETH0_RMII_TX_EN		DCI_D3	TLI_B3	EVENTOUT
PG12				OSPIM_P1_CSN		SPI5_MISO		USART5_RTS/USART5_DE	RSPDIF_CH1	TLI_B4	SDIO1_D3	ETH0_RMII_TXD1	EXMC_NE3	TIMER22_CH0	TLI_B1	EVENTOUT
PG13	TRACED0					SPI5_SCK/I2S5_CK		USART5_CTS	TIMER44_CH0		SDIO1_D6	/ETH0_RMII_TXD0	EXMC_A24	TIMER22_CH1	TLI_R0	EVENTOUT
PG14	TRACED1					SPI5_MOSI/I2S5_SD		USART5_TX	TIMER44_MCH0	OSPIM_P0_IO7	SDIO1_D7	ETH0_RMII_TXD1	EXMC_A25	TIMER22_CH2	TLI_B0	EVENTOUT
PG15								USART5_CTS	TIMER44_BRKIN0				EXMC_SDNCAS	DCI_D13		EVENTOUT

Table 2-13. Port H alternate functions summary

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH0																EVENTOUT

Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
PH1																EVENTOUT

Notes:

(1) Functions are available on GD32H757Zx devices only.

3. Functional description

3.1. Arm® Cortex®-M7 core

The Arm® Cortex®-M7 processor is a highly efficient high-performance, embedded processor that features low interrupt latency, low-cost debug, and has backwards compatibility with existing Cortex-M profile processors. The processor has an in-order super-scalar pipeline that means many instructions can be dual-issued, including load/load and load/store instruction pairs because of multiple memory interfaces. The Cortex-M7 is a high-performance processor, which features a 6-stage superscalar pipeline with branch prediction and an optional FPU capable of single-precision and optionally double-precision operations. The instruction and data buses have been enlarged to 64-bit wide over the previous 32-bit buses.

The interfaces that the processor supports include:

- 64-bit AXI4 interface.
- 32-bit AHB master interface.
- 32-bit AHB slave interface.
- 64-bit instruction TCM interface.
- 2x32-bit data TCM interfaces.

The processor contains the following external interfaces:

- AHBP interface.
- AHBS interface.
- AHBD interface.
- External Private Peripheral Bus.
- ATB interfaces.
- TCM interface.
- Cross Trigger interface.
- MBIST interface.
- AXIM interface.

32-bit Arm® Cortex®-M7 processor core

- Up to 600 MHz operation frequency.
- Single-cycle multiplication and hardware divider.
- Integrated DSP instructions.
- 24-bit SysTick timer.

The Cortex®-M7 processor is based on the ARMv7-M architecture and supports a powerful and scalable instruction set including general data processing I/O control tasks, advanced data processing bit field manipulations, DSP and floating point instructions. Some system peripherals listed below are also provided by Cortex®-M7:

- Nested Vectored Interrupt Controller (NVIC).

- Flash Patch and Breakpoint (FPB).
- Data Watchpoint and Trace (DWT).
- Instrumentation Trace Macrocell (ITM).
- Embedded Trace Macrocell (ETM).
- JTAG or SWD Debug Port.
- Trace Port Interface Unit (TPIU).
- Memory Protection Unit (MPU).
- Floating Point Unit (FPU), double-precision.
- Load Store Unit (LSU).
- Data Processing Unit (DPU).
- Prefetch Unit (PFU).

3.2. On-chip memory

- Up to 3840KB of on-chip flash memory for instruction and data.
- Up to 512 KB of configurable SRAM for ITCM/DTCM/AXI SRAM.
- Up to 512 KB of on-chip SRAM (AXI SRAM).
- 4KB of backup SRAM.
- RAM ECC monitor for each Region.

The GD32H757xx has up to 3840KB of on-chip flash memory for instruction and data. The flash memory consists of 3840KB main flash organized into 960 sectors with 4KB and 64KB information block. Each sector can be erased individually.

The GD32H757xx series contain up to 512KB of on-chip SRAM (AXI SRAM), 4KB of backup SRAM and up to 512KB RAM shared by ITCM/DTCM/AXI SRAM. All of AHB SRAM support byte, half-word (16 bits), and word (32 bits) accesses. The on-chip SRAM (AXI SRAM) support byte, half-word (16 bits), word (32 bits) and double words (64 bits) accesses. SRAM0 and SRAM1 can be accessed by almost all AHB masters. The backup SRAM (BKPSRAM) is implemented in the backup domain, which can keep its content even when the V_{DD} power supply is down.

Table 2-2. GD32H757xx memory map shows the memory map of the GD32H757xx series of devices, including Flash, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 64 MHz factory-trimmed RC and external 4 to 50 MHz crystal oscillator.
- Internal 48 MHz RC oscillator.
- Low power internal 4 MHz RC oscillator.
- Internal 32 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator.
- Integrated system clock PLL.
- 1.71 to 3.6V application supply and I/Os.
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage

detector (LVD).

The Clock Control Unit (CCTL) provides a range of oscillator and clock functions. These include internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AXI, three AHB and four APB domains. The maximum frequency of the system clock can be up to 600 MHz. The maximum frequency of the three AHB domains are 300 MHz. The maximum frequency of the four APB domains including APB1 = APB3 = PAB4 is 150 MHz and APB2 is 300 MHz. See ***Figure 2-5. GD32H757xx clock tree*** for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components except for the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 1.53V and down to 1.48V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 1.71V to 3.6V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} range: 1.71V to 3.6V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} range: 1.71V to 3.6V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

GD32H757xx supports four BOOT modes, including:

- USER BOOT
- SECURITY BOOT
- SYSTEM BOOT
- SRAM BOOT

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDR0/1 in Boot address, allowing to program any boot memory address from 0x0000 0000 to to 0x9000 0000.

The boot loader is located in non-user System memory. It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART1 (PA2 and PA3), USART2 (PB10 and PB11), USBHS0 (USBHS0_DP and USBHS0_DM) and SDIO0 (PC12, PD2, PB13, PC9, PC10 and PC11) in device mode. It also can be used to transfer and update the Flash memory code, the data and the vector table sections.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep** mode
  In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt / event can wake up the system.
- **Deep-sleep** mode
  In deep-sleep mode, all clocks in the 0.9V domain are off, and all of LPIRC4M, IRC64M, HXTAL and PLLs are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, RTC tamper and timestamp event, LXTAL clock stuck, the LVD \ LVD \ OVD, CMP output, LPDTS wakeup, ENET wakeup, RTC wakeup, CAN wakeup, I2C wakeup, USART0 wakeup and USBHS wakeup. When exiting the deep-sleep mode, the IRC64M is selected as the system clock.
- **Standby** mode
  In standby mode, the whole 0.9V domain is power off, the LDO is shut down, and all of LPIRC4M, IRC64M, HXTAL and PLLs are disabled. The contents of SRAM and registers in 0.9V power domain are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC, the FWDGT reset, WKUP pins and LCKMD.

3.6. Electronic fuse (EFUSE)

- One-time programmable nonvolatile efuse storage cells organized as 32*32 bits.
- Double-bit redundant backup mechanism.
- All bits in the efuse cannot be rollback from 1 to 0.
- Each bit in efuse macro can only be programmed once, and software must avoid reprogramming.
- Voltage range for program: 1.71~1.98 V.
- Voltage range for read: 0.72~1.05 V.

The Efuse controller has efuse macro that store system parameters. As a non-volatile unit of storage, the bit of efuse macro cannot be restored to 0 once it is programmed to 1.

3.7. Trigger selection controller (TRIGSEL)

- Supports different optional trigger inputs.
- Trigger input source could be external input signal or output of peripheral.
- Trigger selection output could be for external output or peripheral.

The trigger selection controller (TRIGSEL) allows software to select the trigger input signal for various peripherals. TRIGSEL provides a flexible mechanism for a peripheral to select different trigger inputs. It's up to 4 trigger selection outputs could be selected for each peripheral. And every output could select from different trigger input signal.

3.8. General-purpose and alternate-function I/Os (GPIO and AFIO)

- Up to 135 fast GPIOs, all mappable on 16 external interrupt lines, each pin weak pull-up/pull-down function.
- Output push-pull/open drain enable control.
- Analog input/output configuration.
- Alternate function input/output configuration.

GD32H757xx is up to 113 general purpose I/O pins (GPIO), named PA0~PA10, PA13~PA15, PB0~PB15, PC0~PC15, PD0~PD15, PE0~PE15, PF0~PF15, PG0~PG15, PH0~PH1 for the device to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the Interrupt/Event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog mode.

3.9. CRC calculation unit (CRC)

- Supports 7/8/16/32 bit data input.
- For 7(8)/16/32 bit input data length, the calculation cycles are 1/2/4 AHB clock cycles.
- User configurable polynomial value and size.
- Free 8-bit register is unrelated to calculation and can be used for any other goals by any other peripheral devices.

A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. The CRC calculation unit can be used to calculate 7/8/16/32 bit CRC code within user configurable polynomial.

3.10. True random number generator (TRNG)

- LFSR mode and NIST mode to generate random number (National Institute of Standards and Technology) mode to generate random number.
- About 40 periods of TRNG_CLK are needed between two consecutive random numbers

in LFSR mode.

- 32-bit random numbers are generated each time in LFSR mode.
- TRNG NIST mode follows the NIST SP800-90B.
- Support health tests recommended by the NIST SP800-90B.
- 32-bit*4 or 32-bit*8 random numbers are generated each time in NIST mode.
- TRNG has the functions of startup and in-service self-check, associated with specific error flags.
- 128-bit random value seed is generated from analog noise.

The true random number generator (TRNG) module can generate a 32-bit random value by using continuous analog noise and it has been pre-certified NIST SP800-90B.

3.11. Cryptographic Acceleration Unit (CAU)

- Supports DES, TDES or AES (128, 192, or 256) algorithms.
- DES/TDES supports Electronic codebook (ECB) or Cipher block chaining (CBC) mode.
- AES supports 128bits-key, 192bits-key or 256 bits-key.
- Multiple modes are supported respectively in DES, TDES and AES, including Electronic codebook (ECB), Cipher block chaining (CBC), Counter mode (CTR), Galois / counter mode (GCM), Galois message authentication code mode (GMAC), Counter with CBC-MAC (CCM), Cipher Feedback mode (CFB) and Output Feedback mode (OFB).
- DMA transfer for incoming and outgoing data is supported.

The cryptographic acceleration unit (CAU) is used to encipher and decipher data with DES, Triple-DES or AES (128, 192, or 256) algorithms. DES / TDES / AES algorithms with different key sizes are supported to perform data encryption and decryption in the CAU in multiple modes. The CAU is a 32-bit peripheral, DMA transfer is supported and data can be accessed in the input and output FIFO.

3.12. Hash Acceleration Unit (HAU)

- Federal Information Processing Standards Publication 180-4(FIPS PUB 180-4).
- Secure Hash Standard specifications (SHA-1, SHA-224, SHA-256).
- Internet Engineering Task Force Request for Comments number 1321 (IETF RFC 1321) specifications (MD5).
- High performance of computation of hash algorithms.
- Automatic data padding to fill the 512-bit message block for digest computation.
- DMA transfer is supported.
- Hash / HMAC process suspended mode.

The hash acceleration unit (HAU) is used for information security. The secure hash algorithm (SHA-1, SHA-224, SHA-256), the message-digest algorithm (MD5) and the keyed-hash message authentication code (HMAC) algorithm are supported for various applications. The digest will be computed and the length is 160 / 224 / 256 / 128 bits for a message up to (264

- 1) bits computed by SHA-1, SHA-224, SHA-256 and MD5 algorithms respectively. In HMAC algorithm, SHA-1, SHA-224, SHA-256 or MD5 will be called twice as hash functions and authenticating messages can be produced.

3.13. Trigonometric Math Unit (TMU)

- 10 kinds of functions.
- The fixed point format is configurable.
- Programmable precision.
- CORDIC-algorithm core: circular system and hyperbolic system, rotation pattern and vectoring pattern.

The Trigonometric Math Unit (TMU) is a fully configurable block that execute common trigonometric and arithmetic operations. It can be used to calculate total 10 kinds of functions. The input/output data meet q1.31 or q1.15 fixed point format.

3.14. Direct memory access controller (DMA)

- Two AHB master interface for transferring data, and one AHB slave interface for programming DMA.
- 16 channels (8 for DMA0 and 8 for DMA1) and each channel are configurable.
- Support independent single, 4, 8, 16-beat incrementing burst memory and peripheral transfer.
- Support independent 8, 16, 32-bit memory and peripheral transfer.
- Peripherals supported: Timers, ADC, HPDF, SPI, I2C, USART, UART, DAC, I2S, RSPDIF, SAI, CAU, HAU, FAC, TMU, CAN and DCI.

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Two AHB master interfaces and eight four-word depth 32-bit width FIFOs are presented in each DMA controller, which achieves a high DMA transmission performance. There are 16 independent channels in the DMA controller (8 for DMA0 and 8 for DMA1). Each channel is assigned a specific or multiple target peripheral devices for memory access request management. Two arbiters respectively for memory and peripheral are implemented inside to handle the priority among DMA requests.

3.15. Master direct memory access controller (MDMA)

- 16 channels, each channel supports software triggering and requests can be selected among any request source.

- Support independent single, 2, 4, 8, 16, 32, 64, 128-beat incrementing burst source and destination transfer.
- Support three transfer modes:
  - Read from memory and write to memory (software triggered).
  - Read from peripheral and write to memory (or memory mapped peripherals).
  - Read from memory (or memory mapped peripherals) and write to peripheral.
- Automatic pack / unpack of data to optimize bandwidth when the data width of the source and destination are different.
- 34 hardware trigger sources, all channels can be connected to any hardware trigger source.
- Two FIFOs of 16 double word depth to maximize data bandwidth and bus utilization.

The master direct memory access (MDMA) controller provides a hardware method of transferring data between peripherals and/or memory without intervention from the MCU, thereby increasing system performance by off-loading the MCU from copying large amounts of data and avoiding frequent interrupts to serve peripherals needing more data or having available data. MDMA can be used in combination with a DMA controller (DMA0 or DMA1) to provide up to 16 channels. Each channel request can be selected among any request source. The built-in arbiter is used to handle priority among MDMA requests.

3.16. DMA request multiplexer (DMAMUX)

- 16 channels for DMAMUX request multiplexer.
- 8 channels for DMAMUX request generator.
- Support 36 trigger inputs and 29 synchronization inputs.

DMAMUX is a transmission scheduler for DMA requests. The DMAMUX request multiplexer is used for routing a DMA request line between the peripherals / generated DMA request (from the DMAMUX request generator) and the DMA controller. Each DMAMUX request multiplexer channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. The DMA request is pending until it is served by the DMA controller which generates a DMA acknowledge signal (the DMA request signal is de-asserted).

3.17. Analog to digital converter (ADC)

- 14-bit ADC0 and ADC1 conversion rate is up to 4 MSPS.
- 12-bit ADC2 conversion rate is up to 5.3 MSPS.
- 14-bit,12-bit, 10-bit, 8-bit configurable resolution for ADC0 and ADC1.
- 12-bit, 10-bit, 8-bit or 6-bit configurable resolution for ADC2.
- In ADC0 and ADC1, Oversampling ratio arbitrarily adjustable from 2x to 1024X.
- ADC2, Oversampling ratio arbitrarily adjustable from 2x to 256X.
- ADC0 and ADC1 supply requirements: 1.8V to 3.6V, and typical power supply voltage is

3.3V, ADC2 supply requirements: 1.71V to 3.6V, typical power supply voltage is 3.3V.

- ADC input voltage range: $V_{REFN} \le V_{IN} \le V_{REFP}$.
- Temperature sensor.
- Start-of-conversion can be initiated by software or TRIGSEL.

A 12 / 14-bit successive approximation analog-to-digital converter module (ADC) is integrated on the MCU chip. ADC0 has 20 external channels, 1 internal channel (DAC_OUT0 channel), ADC1 has 18 external channels, 3 internal channels (the battery voltage, V_{REFINT} inputs channel and DAC_OUT1 channel), ADC2 has 17 external channels, 4 internal channels (the battery voltage, V_{REFINT} inputs channel, tempeture sensor and high-precision tempeture sensor). After sampling and conversion, the conversion results can be stored in the corresponding data registers according to the least significant bit (LSB) alignment or the most significant (MSB) bit alignment (ADC0 / 1 are 32-bit data register, ADC2 is 16-bit data register). An on-chip hardware oversample scheme improves performances and reduces the computational burden of MCU.

3.18. Digital to analog converter (DAC)

- 8-bit or 12-bit resolution. Left or right data alignment.
- Conversion update synchronously.
- Conversion trigged by external triggers.
- Input voltage reference, V_{REFP}.
- Output buffer calibration.
- Using sample and keep mode to reduce the power consumption.
- Noise wave generation (LFSR noise mode and Triangle noise mode).
- Two DAC channels in concurrent mode.

The Digital-to-analog converter converts 12-bit digital data to a voltage on the external pins. The digital data can be set to 8-bit or 12-bit mode, left-aligned or right-aligned mode. DMA can be used to update the digital data on external triggers. The output voltage can be optionally buffered for higher drive capability, and DAC output buffer can be calibrated to improve output accuracy. The sample and keep mode can reduce the power consumption of DAC.

3.19. Real time clock (RTC) and backup registers

- Support calendar function, which can support year, month, date, day, hours, minutes, seconds and subseconds (date is the day of week and day is the day of month).
- Daylight saving compensation supported, which is realized through software.
- External high-accurate low frequency (50Hz or 60Hz) clock used to achieve higher calendar accuracy performed by reference clock detection option function.
- Atomic clock adjust (max adjust accuracy is 0.95PPM) for calendar calibration performed by digital calibration function.

- Sub-second adjustment by shift function.

The RTC provides a time which includes hour/minute/second/sub-second and a calendar includes year/month/day/week day. The time and calendar are expressed in BCD code except sub-second. Sub-second is expressed in binary code. Hour adjust for daylight saving time.

The RTC is an independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. A prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.20. Timers and PWM generation

- Two 16-bit Advanced timer (TIMER0 & TIMER7), four16-bit General-L0 timers (TIMER2, TIMER3, TIMER30, TIMER31), four 32-bit General-L0 timers (TIMER1, TIMER4, TIMER22, TIMER23), six 16-bit General-L3 timers (TIMER14, TIMER40, TIMER41, TIMER42, TIMER43, TIMER44), two16-bit General-L4 timers (TIMER15, TIMER16), two 32-bit Basic timer (TIMER5 & TIMER6) and two 64-bit Basic timer (TIMER50 & TIMER51).
- Up to 70 independent channels of PWM, output compare or input capture for each general timer and external trigger input.
- 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match.
- Encoder interface controller with two inputs using quadrature decoder and non-quadrature decoder mode.
- 24-bit SysTick timer down counter.
- 2 watchdog timers (free watchdog timer and window watchdog timer).

The advanced timer (TIMER0 & TIMER7) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general timer. The 8 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned counting modes) and single pulse mode output. If configured as a general 16-bit timer, it has the same functions as the TIMERx timer. It can be synchronized with external signals or to interconnect with other general timers together which have the same architecture and features.

The general level 0 timer, can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1/4/22/23 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2/3/30/31 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. The general level 0 timer also supports an encoder interface with two inputs using quadrature decoder mode and non-quadrature decoder mode.

The general level3 timer module (TIMER14/40/41/42/43/44) is a three-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level3 timer has a 16-bit counter that can be used as an unsigned counter.

The general level4 timer module (TIMER15/16) is a two-channel timer that supports both input capture and output compare. They can generate PWM signals to control motor or be used for power management applications. The general level4 timer has a 16-bit counter that can be used as an unsigned counter.

The basic timer module(TIMER5/6/50/51) has a 32-bit or 64-bit counter that can be used as an unsigned counter. The basic timer can be configured to generate a DMA request and a TRGO0 to connect to DAC.

The GD32H757xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 32 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter.
- Auto reload capability.
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source.

3.21. Universal synchronous/asynchronous receiver transmitter (USART/UART)

- Programmable baud-rate generator allowing speed up to 37.5 MBits/s when the clock frequency is 300 MHz and oversampling is by 8.
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support.
- LIN break generation and detection.
- ISO 7816-3 compliant smart card interface.

The USART (USART0, USART1, USART2, USART5) and UART (UART3, UART4, UART6, UART7) are used to transfer data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART/UART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART/UART transmitter and receiver.

3.22. Inter-integrated circuit (I2C)

- Up to three I2C bus interfaces can support both master and slave mode with a frequency up to 1 MHz (Fast mode plus).
- Provide arbitration function, optional PEC (packet error checking) generation and checking.
- Supports 7-bit and 10-bit addressing mode and general call addressing mode.
- SMBus 3.0 and PMBus 1.3 compatible.
- Wakeup from sleep mode and Deep-sleep mode on I2C address match.

The I2C (inter-integrated circuit) module provides an I2C interface which is an industry standard two-line serial interface for MCU to communicate with external I2C interface. I2C bus uses two serial lines: a serial data line, SDA, and a serial clock line, SCL. The I2C interface implements standard I2C protocol with standard mode (up to 100KHz), fast mode (up to 400KHz) and fast mode plus (up to 1MHz) as well as CRC calculation and checking, SMBus (system management bus), and PMBus (power management bus).

3.23. Serial peripheral interface (SPI)

- Master or slave operation with full-duplex, half-duplex or simplex mode.
- Separate transmit and receive 32-bit FIFO.
- Data frame size can be 4 to 32 bits.
- Hardware CRC calculation, transmission and checking.
- SPI TI mode supported.
- Multi-master or multi-slave mode function.
- Protect configurations and settings.
- Adjustable main device receiver sampling time.
- Configurable FIFO thresholds (data packing).
- Quad-SPI configuration available in master mode (in SPI3 / 4).

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking. Quad-SPI master mode is also supported in SPI3 and SPI4.

3.24. Inter-IC sound (I2S)

- Master or slave operation for transmission/reception.
- Four I2S standards supported: Phillips, MSB justified, LSB justified and PCM standard.
- Data length can be 16 bits, 24 bits or 32 bits.
- Channel length can be 16 bits or 32 bits.
- Transmission and reception use a 32 bits wide buffer.
- Audio sample frequency can be 8 kHz to 192 kHz using I2S clock divider.
- Programmable idle state clock polarity.
- Separate transmit and receive 32-bit FIFO.

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 4-wire serial lines. GD32H757xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequencies from 8 KHz to 192 KHz is supported.

3.25. OSPI I/O manager(OSPIM)

- Supports two OSPI (single-line, two-lines, four-lines, eight-lines) interfaces.
- Support two ports for pin assignment.
- Fully programmable IO matrix, can assign pins according to function.

OSPIM supports OSPI pin assignment with full matrix.

3.26. Octal-SPI interface(OSPI)

- Three functional modes: indirect mode, status polling mode, memory-mapped mode.
- Support read in memory-mapped mode.
- Support single, dual, quad and octal communication.
- Fully programmable command format for both indirect and memory-mapped mode.
- Support SDR (signal data rate) and DTR (double transfer rate, only for GD25LX512ME).
- Integrated FIFO for transmission/reception.
- 8, 16 and 32-bits data access.

The OSPI is a specialized interface that communicate with external memories. The interface support single, dual, quad and octal SPI flash (PSRAMS, NAND, NOR Flash, etc).

3.27. Clock phase delay module (CPDM)

- Supports the input clock frequency ranges: 25 MHz ~ 208MHz.
- Supports up to 12 oversampling phases.

The Clock Phase Delay Module (CPDM) is used to delay the phase of the input clock and then output the clock. When used, the application needs to first program the phase of the output clock, and then use the output clock in other peripherals to receive data.

Phase delay is related to voltage and temperature and may require reconfiguration of the application and redetermination of the phase relationship between the output clock and the received data as parameters change.

3.28. Digital camera interface (DCI)

- Digital video/picture capture.
- 8/10/12/14 data width supported.
- High transfer efficiency with DMA interface.
- Video/picture crop supported.
- Various pixel digital encoding formats supported including YCbCr422 / RGB565 / YUV420 / Bayer.
- Hard/embedded synchronous signals supported.
- Support for CCIR656 video interface as well as traditional sensor interface.

DCI is an 8-bit to 14-bit parallel interface that able to capture video or picture from a camera via Digital Camera Interface. It supports 8/10/12/14 bits data width through DMA operation.

DCI supports various color space such as YUV/RGB, as well as compression format such as JPEG. Support CCIR656 video decoder formats and perform additional processing of the image.

3.29. TFT LCD interface (TLI)

- Supports up to 24 bits data output per pixel.
- Supports up to 2048 x 2048 resolution.
- Support various pixel formats: ARGB8888, RGB888, RGB565, etc.
- Support CLUT (Color Look-Up-Table) and Color-Keying format.

The TFT LCD interface provides a parallel digital RGB (Red, Green and Blue) and signals for horizontal, vertical synchronization, pixel clock and data enable as output to interface directly to a variety of LCD (Liquid Crystal Display) and TFT (Thin Film Transistor) panels. A built-in DMA engine continuously move data from system memory to TLI and then, output to an external LCD display. Two separate layers are supported in TLI, as well as layer window and blending function.

3.30. Receiver of Sony/Philips Digtial Interface (RSPDIF)

- Supports audio IEC-60958 and IEC-61937.
- Up to 4 inputs available.
- Supports maximum symbol rate: 12.288 MHz.

- Supports stereo stream from 8 to 192 kHz.
- Supports automatic symbol rate detection.
- Genrate symbol clock.
- Check the parity bit of the received data.
- Support multiple data processing methods, which can process audio data and user channel information separately or together.
- Supports using DMA communication to receive audio data and user channel information respectively.

The receiver of Sony/Philips Digital Interface (RSPDIF) module provides the function of receiving and decoding RSPDIF audio data streams.

3.31. Serial Audio Interface (SAI)

- Two independent audio sub-blocks.
- Each audio sub-block can be configured as any of the master/slave and transmitter/receiver combination with 8-word FIFO.
- Local clock divider logic to satisfy the various audio sampling rates.
- Flexible audio protocol configuration such as I2S, PCM/DSP, AC’97, LSB or MSB-justified and TDM.
- PDM interface, supporting up to 3 microphone pairs.
- Mono/Stereo audio capability with mute option.
- Frame Synchronization configuration (active level, active length and offset).
- Each audio frame contains up to 16 configurable slots.
- Slot length is flexible, and can be configured as active or inactive.
- Each slot can hold a data of size 8-, 10-, 16-, 20-, 24-, and 32-bits with configurable first bit offset, and configurable LSB or MSB data transfer.
- Two independent DMA interface for each audio sub-block. Support slave mode with a frequency up to 4MHz.

The Serial Audio Interface (SAI) is designed to target a wide range of commonly used audio protocols, both in mono and stereo modes, such as I2S, PCM/DSP, AC’97, LSB or MSB-justified and TDM. SPDIF output is offered when the audio block is configured as a transmitter. The SAI can be configured to any of the master/slave and transmitter/receiver combination, full/half-duplex operating mode depends on synchronous/asynchronous configuration of the audio sub-blocks.

3.32. Image processing accelerator (IPA)

- Copy one source image to the destination image.
- Convert one source image to the destination image with specific pixel format.
- Convert and blend two source images to the destination image with specific pixel format.
- Fill up the destination image with a specific color.

The IPA provides a configurable and flexible image format conversion from one or two source image to the destination image. Sixteen pixel formats for foreground from 4-bit up to 32-bit per pixel, eleven pixel formats for background from 4-bit up to 32-bit per pixel, and five pixel formats from 16-bit up to 32-bit per pixel for the destination image are supported. Two 256*32 bits LUTs (Look-Up Table) separately for the two source images are implemented for the indirect pixel formats.

3.33. Secure digital input and output card interface (SDIO)

- ***e*•MMC:** Support for embedded Multimedia Card System Specification Version 4.51 (and previous versions) Card and five different data bus modes: 1-bit (default), 4-bit (SDR/DDR) and 8-bit(SDR/DDR).
- **SD Card:** Full support for SD Memory Card Specifications Version 3.0.
- **SD I/O:** Full support for SD I/O Card Specification Version 3.0 card and three different data bus modes: 1-bit (default) and 4-bit (SDR/DDR).
- 104MHz data transfer frequency and 8-bit data transfer mode.
- Support DDR and max clock frequency is 50Mhz.

The secure digital input/output interface (SDIO) defines the SD, SD I/O and embedded MultiMediaCard (e•MMC) host interface, which provides command/data transfer between the AHB system bus and SD memory cards, SD I/O cards and e•MMC.

3.34. Management data input/output (MDIO)

- Support slave mode with a frequency up to 4MHz.
- Support CFP/CFP2 MSA Management Interface Specification.

The MDIO interface can receive complete MDIO frames. As long as the data is written to the register before receiving the turnaround bits (TA) of the read or post read increment address frame, the MDIO interface can transmit complete MDIO frames. Interrupts are generated at the end of every complete frame, which can be used or provided at correct time. Interrupts can also be generated after every valid PHYADR and DEVADD, which allows more complex controls within frames.

3.35. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM, NOR-Flash, 8/16-bit NAND Flash and Synchronous DRAM (SDRAM).
- Embedded ECC hardware for NAND Flash access.
- Two SDRAM banks with independent configuration, up to 13-bits Row Address, 11-bits Column Address, 2-bits internal banks address.
- SDRAM Memory size: 4x16Mx32bit (256 MB), 4x16Mx16bit (128 MB), 4x16Mx8bit (64 MB).

The external memory controller EXMC, is used as a translator for CPU to access a variety of external memory, it automatically converts AXI memory access protocol into a specific memory access protocol defined in the configuration register, such as SRAM, ROM, NOR Flash, PSRAM, NAND Flash and SDRAM. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.36. VREF

- Stable voltage, and product calibrated.
- Connects to VREFP pin to source off-chip circuits.
- 1.5V, 1.8V, 2.048V or 2.5V configurable reference voltage output.

A precision internal reference circuit is inside. The internal voltage reference unit is used to provide voltage reference for ADC / DAC, or used by off-chip circuit connecting to VREFP pin.

3.37. Low power digital temperature sensor (LPDTS)

- The trigger source of measurement can be set to software or hardware.
- Programmable sampling time.
- Temperature window watchdog.
- The interrupt can be generated when the temperature is below a low threshold or above a high threshold and at the end of measurement.
- The generation of asynchronous wakeup signal in LXTAL mode indicates that the measurement result is higher or lower than the specified threshold.

Low power digital tempearature sensor(LPDTS) is used to transmit square wave, which is converted by temperature and the frequency is proportional to the absolute temperature. The frequency measurement is based on the PCLK or the LXTAL clock.

3.38. Encoder Divided-Output controller (EDOUT)

- Support for changing the activation polarity of B.
- Support configuration of Z-phase output location and pulse width.
- Number of edges per rotation: 16 to 65536 (must be the multiple of four).
- Support for the input of update period event signals from the TRIGSEL.

The encoder divided-output controller (EDOUT) is used to output location information obtained from the encoder in the form of A-phase, B-phase, and Z-phase pulses.

3.39. Controller area network (CAN)

- Supports CAN protocol version 2.0A/B.

- Compliant with the ISO 11898-1:2015 standard.
- Supports CAN FD frame with up to 64 data bytes, baudrate up to 8 Mbit/s.
- Supports CAN classical frame with up to 8 data bytes, baudrate up to 1 Mbit/s.
- Supports time stamp based on 16-bit free running counter.
- Supports transmitter delay compensation for CAN FD frames at faster data rates.
- Maskable interrupts.
- Supports four communication mode: normal mode, Inactive mode, Loopback and silent mode, and Monitor mode.
- Supports two power saving modes: CAN_Deepsleep mode, and CAN_sleep mode.
- Support two wakeup methods for waking up from Pretended Networking mode: wakeup matching event, and wakup timeout event.
- Global network time, synchronized by a specific message.

CAN bus (Controller Area Network) is a bus standard designed to allow microcontrollers and devices to communicate with each other without a host computer. The CAN interface supports the CAN 2.0A/B protocol, ISO 11898-1:2015 and BOSCH CAN FD specification.

The CAN module is a CAN Protocol controller with a very flexible mailbox system for transmitting and receiving CAN frames. The mailbox system consists of a set of mailboxes that store configuration and control data, timestamp, message ID, and data. The space of up to 32 mailboxes can also be configured as Rx FIFO with ID filtering against up to 104 extended IDs or 208 standard IDs or 416 partial 8-bit IDs, and configure receive FIFO/mailbox private filter register for up to 32 ID filter table elements.

3.40. Ethernet (ENET)

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN.
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM.
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588.

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via a reduced media independent interface (RMII). The number of RMII signals provided up to 7 with 50 MHz output. The function of 32-bit CRC checking is also available.

3.41. Comparator (CMP)

- Rail-to-rail comparators.
- Configurable hysteresis.
- Configurable speed and consumption.
- Each comparator has configurable analog input source.
- Outputs with blanking source.
- Outputs to I/O.

- Outputs to timers for capture.
- Outputs to EXTI and NVIC.

The general purpose comparators, CMP0 and CMP1, can work either standalone (all terminal are available on I/Os) or together with the timers. It could be used to wake up the MCU from low-power mode by an analog signal, provide a trigger source when an analog signal is in a certain condition, achieves some current control by working together with a PWM output of a timer and the DAC. It blanking function can be used for false overcurrent detection in motor control applications.

3.42. High-Performance Digital Filter (HPDF)

- 8 multiplex digital serial input channels.
  - configurable SPI and Manchester interfaces.
- 8 internal digital parallel input channels.
  - input with up to 16-bit resolution.
  - internal source: ADC data or memory (CPU/DMA write) data stream.
- Configurable Sinc filter and integrator.
  - the order and oversampling rate (decimation rate) of Sinc filter can be configured.
  - sampling rate of configurable integrator.
- Threshold monitor function.
  - independent Sinc filter, configurable order and oversampling rate (decimation rate).
  - configurable data input source: serial channel input data or HPDF output data.
- Malfunction monitor function.
  - A counter with 8 bits is used to monitor the continuous 0 or 1 in the serial channel input data stream.
- Extreme monitor function.
  - store minimum and maximum values of output data values of HPDF.
- Up to 24-bit output data resolution.
- Clock signal can be provided to external sigma delta modulator.
  - provide configurable clock signal by the CKOUT pin.
- HPDF output data is in signed format.

A high performance digital filter module (HPDF) for external sigma delta (Σ-Δ) modulator is integrated in GD32H757xx. HPDF supports SPI interface and Manchester-coded single-wire interface. The external sigma delta modulator can be connected with MCU by the serial interface, and the serial data stream output by sigma delta modulator can be filtered. In addition, HPDF also supports the parallel data stream input, which can be selected from internal ADC peripherals or from MCU memory.

3.43. Real-time decryption (RTDEC)

- Software configurable encrypted areas up to 4.

- Granularity is 4096 bytes in RTDEC programmed areas.
- Every area can be configured the independent 128-bits key, 16-bits area firmware version, and 64-bits application-defined nonce.
- Confidentiality and completeness protection for encryption keys.
  - 128-bits key registers are write-only, with software locking mechanism.
  - 8-bits CRC is calculated automatically by hardware, and it’s used as the public key information.
- The real-time decryption when OSPI memory-mapped read operations.
  - Use of AES-128 in CTR mode.
  - Support key stream FIFO with depth 4.
  - Support various read size.
  - Decryption / encryption with physical address of the reads.
- Support for GD32 OSPI pre-fetching mechanism.

The real-time decryption (RTDEC) allows to decrypt in real-time according to information of the read request address. RTDEC can configure four independent and different encrypted areas. And each area has the option of execute-only or execute-never enforcement to choose.

For real-time performance, RTDEC uses the counter (CTR) mode of AES-128. Since RTDEC using AES in counter mode, the whole area has to be re-encrypted with an updated cryptographic context (key or initialization vector) when the data or code of one encrypted area is changed. This feature makes RTDEC only suitable for decrypting read-only content, like that stored in external flash.

3.44. Filter arithmetic accelerator (FAC)

- Fixed or float multiplier and accumulator.
- 256 x 32-bit local memory.
- 16-bit fixed-point or 32-bit float point input and output.
- Up to three buffers, two input buffers and one output buffer.
- Buffer can be circular.
- FIR and IIR can be realized.
- Vector functions support convolution, Dot product, correlation functions.
- Data can be read and written through DMA.

The filter arithmetic accelerator unit consist of multiplier, accumulator and address generation logic, so as to index vector elements stored in local memory. Circular buffering is valid for both input and output, which allows to realize finite impulse response (FIR) filters and infinite impulse response (IIR) filters. The unit support CPU to be free from frequent or lengthy filtering operations, compared with software implementation, it can accelerate calculations and the processing speed of time critical tasks.

3.45. Hardware semaphore (HWSEM)

- 32 semaphores.
- An interrupt is generated when a semaphore is unlocked.
- Semaphore is unlocked only when MID[3:0] and PID[7:0] are matched.

Hardware semaphore (HWSEM) provides a non-blocking mechanism to ensure the synchronous of processes. HWSEM realizes 32 semaphores in an atomic way, supporting semaphore write lock and read lock, and semaphore can only be unlocked when bus master and process are matched.

3.46. Universal serial bus high-speed interface (USBHS)

- Supports USB 2.0 Host mode at High-Speed(480Mb/s), Full-Speed(12Mb/s) or Low-Speed(1.5Mb/s).
- Supports USB 2.0 device mode at High-Speed(480Mb/s) or Full-Speed(12Mb/s).
- Supports OTG protocol with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol).

USB High-Speed (USBHS) controller provides a USB-connection solution for portable devices. USBHS supports both host and device modes, as well as OTG mode with HNP (Host Negotiation Protocol) and SRP (Session Request Protocol). USBHS contains an embedded USB PHY internal which can be configured as High-Speed or Full-Speed. USBHS supports all the four types of transfer (control, bulk, Interrupt and isochronous) defined in USB 2.0 protocol. There is also a DMA engine operating as an AHB bus master in USBHS to speed up the data transfer between USBHS and system. For Full-Speed operation, battery charging detection (BCD), attach detection protocol (ADP), and link power management (LPM) are also supported.

3.47. Debug mode

- JTAG and SWD Debug Port.

The GD32H757xx series provide a large variety of debug, trace and test features. They are implemented with a standard configuration of the Arm® CoreSight™ module together with a daisy chained standard TAP controller. Debug and trace functions are integrated into the ARM® Cortex®-M7. The debug system supports serial wire debug (SWD) and trace functions in addition to standard JTAG debug.

3.48. Package and operation temperature

- LQFP144 (GD32H757Zx), BGA100\LQFP100 (GD32H757Vx).

- Operation temperature range: -40°C to +85°C (industrial level).

4. Electrical characteristics

To better understand this chapter, read the following before moving on to the rest of this chapter.

- A + or no sign before the current value indicates that the current is output from the MCU.
- A - before the current value indicates that the current is input to the MCU.
- T_A (Ambient temperature) tested condition.
- T_J (Junction temperature) tested condition.
- Value guaranteed by design, not 100% tested in production indicates that the value is derived from simulation of IC designers.
- Value guaranteed by characterization, not 100% tested in production indicates that the value is derived from random test.
- Unless otherwise specified, all values given for V_{DD} = V_{DDA} = 3.3 V, T_J = 25 °C.
- The devices will be damaged or work abnormally if the electrical parameters beyond the range of maximum and minimum values.

See the following table for some abbreviation terms and their descriptions in this chapter.

Table 4-1. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CAN	Controller Area Network
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
USB	Universal Serial Bus
SPI	Serial Peripheral Interface
RMII	Reduced Media Independent Interface

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-2. Absolute maximum ratings(1)(4)

Symbol	Parameter	Min	Max	Unit
V_{DD}	External voltage range(2)	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage(3)	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
$V_{DD50USB}$	$V_{DD50USB}$ supply voltage	V_{SS} - 0.3	V_{SS} + 5.6	V
V_{IN}	Input voltage on 5VT I/O(5)	V_{SS} - 0.3	V_{DD}+3.6	V
	Input voltage on other I/O	V_{SS} - 0.3	V_{SS} +3.6	
$\|\Delta V_{DDX}\|$	Variations between different V_{DD} power pins	—	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins	—	50	mV
I_{IO}	Maximum current for GPIO pins	—	25	mA
$\sum I_{IO}$	Maximum current sunk/sourced by all GPIO pin	—	120	
I_{DD}	Maximum current into each V_{DD} pin	—	120	
I_{SS}	Maximum current into each V_{SS} pin	—	120	
T_A	Operating temperature range	-40	+85	°C
P_D	Power dissipation at T_A = 85°C of LQFP144	—	847	mW
	Power dissipation at T_A = 85°C of LQFP100	—	836	
	Power dissipation at T_A = 85°C of BGA100	—	813	
T_{STG}	Storage temperature range	-65	+150	°C
T_J	Maximum junction temperature	—	125	°C

(1) Value guaranteed by design, not 100% tested in production.
(2) All main power and ground pins should be connected to an external power source within the allowable range.
(3) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.
(4) The device junction temperature must be kept below maximum T_J. More information could be found in ***AN166 Design Guide for Thermal Characteristics of GD32H7xx series.***
(5) V_{IN} maximum value cannot exceed 5.5 V.

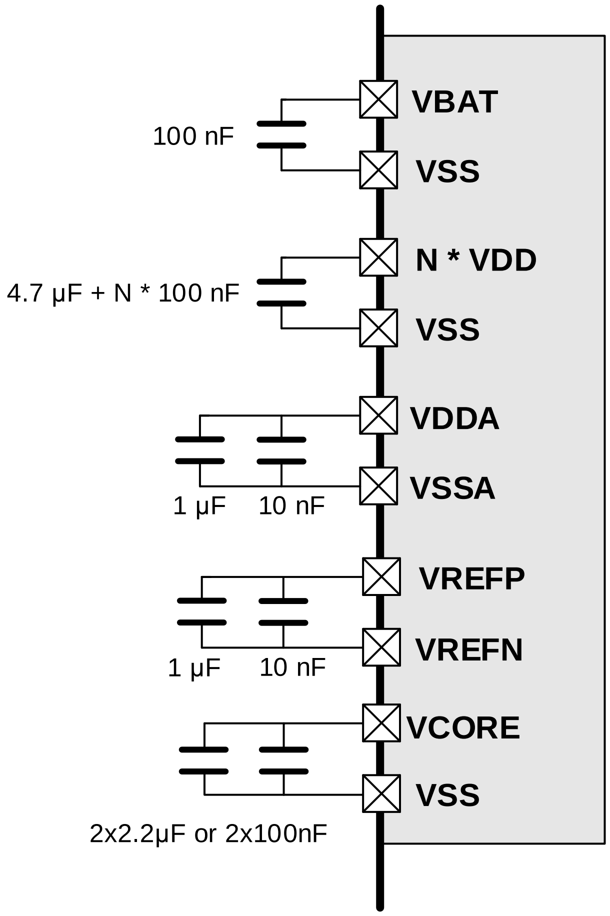
4.2. Recommended DC characteristics

Table 4-3. DC operating conditions

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	Supply voltage	—	1.71	3.3	3.6	V
V_{DDLDO}	Supply voltage for the internal regular	$V_{DDLDO} \leq V_{DD}$	1.71	—	3.6	V
$V_{DD50USB}$	—	USB regulator ON	4.0	5.0	5.5	V
		USB regulator OFF	—	$V_{DD33USB}$	—	V
$V_{DD33USB}$	Standard operating voltage, USB domain	USB used	3.0	—	3.6	V
		USB not used	0	—	3.6	V
V_{DDA}	Analog supply voltage	Same as V_{DD}	1.71	3.3	3.6	V
V_{BAT}	Battery supply voltage	—	1.71	—	3.6	V

(1) Value guaranteed by characterization, not 100% tested in production.

Figure 4-1. Recommended power supply decoupling capacitors(1)(2)(3)



(1) The VREFP and VREFN pins are only available on no less than 100-pin packages, or else the VREFP and VREFN pins are not available and internally connected to VDDA and VSSA pins.

(2) All decoupling capacitors need to be as close as possible to the pins on the PCB board.

(3) When voltage regulator is enabled the two 2.2 µF Vcore capacitors are required , if bypassing the voltage regulator ,two 100 nF decoupling capacitors are required.

Table 4-4. Vcore operating conditions(1)(2)(3)

Symbol	Parameter	Conditions
C_{EXT}	Capacitance of external capacitor	2.2 µF
ESR	ESR of external capacitor	< 100 mΩ

(1) When bypassing the voltage regulator, the two 2.2 µF V_{CORE} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

(2) This value corresponds to C_{EXT} typical value. A variation of +/-20% is tolerated.

(3) If a third V_{CORE} pin is available on the package, it must be connected to the other V_{CORE} pins but no additional capacitor is required.

Table 4-5. Clock frequency(1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	core clock frequency	Supply voltage < 3.6V	—	600	MHz
		Supply voltage < 2.3V	—	400	
f_{AHB}	AHB clock frequency	Supply voltage < 3.6V	—	300	
		Supply voltage < 2.3V	—	200	

f_{APB1}	APB1 clock frequency	—	—	150(2)	
f_{APB2}	APB2 clock frequency	—	—	300(2)	
f_{APB3}	APB3 clock frequency	—	—	150(2)	
f_{APB4}	APB4 clock frequency	—	—	150(2)	

(1) Value guaranteed by design, not 100% tested in production.

(2) APBx clocks are divided from AHB clock.

Table 4-6. TCM interface frequency(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{TWW}	TCM without wait	—	—	350	MHz

(1) Value guaranteed by design, not 100% tested in production.

Table 4-7. Operating conditions at Power up / Power down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	—	0	∞	µs/V
	V_{DD} fall time rate		100	∞	
t_{VDDA}	V_{DDA} rise time rate	—	0	∞	
	V_{DDA} fall time rate		100	∞	
$t_{VDD(USB)}$	$V_{DD(USB)}$ rise time rate	—	0	∞	
	$V_{DD(USB)}$ fall time rate		100	∞	

(1) Value guaranteed by design, not 100% tested in production.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-8. Power consumption characteristics(1)(2)(3)(4)

Symbol	Parameter	Conditions	Typ LDO regulator ON	Max	Unit
$I_{DD}+I_{DDA}$	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals enabled, code run in ITCM	161	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals enabled, code run in Flash and cache on	151	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals enabled, code run in Flash and cache off	151	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals disabled, code run in ITCM	47.5	—	mA

Symbol	Parameter	Conditions	Typ LDO regulator ON	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals disabled, code run in Flash and cache on	52.4		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals disabled, code run in Flash and cache off	52.3		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals enabled, code run in ITCM	110		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals enabled, code run in Flash and cache on	103		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals enabled, code run in Flash and cache off	103		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals disabled, code run in ITCM	36.5		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals disabled, code run in Flash and cache on	39.5		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals disabled, code run in Flash and cache off	39.5		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 64 MHz, All peripherals enabled, code run in ITCM	44.6		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 64 MHz, All peripherals enabled, code run in Flash and cache on	43.9		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 64 MHz, All peripherals disabled, code run in ITCM	20.5		mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 64 MHz, All peripherals disabled, code run in Flash and cache on	20.5		mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals enabled	151	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 600 MHz, All peripherals disabled	49.2	—	mA
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals enabled	104	—	mA

Symbol	Parameter	Conditions	Typ LDO regulator ON	Max	Unit
		V_{DD} = V_{DDA} = 3.3 V, System clock = 400 MHz, All peripherals disabled	37.5	—	mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO=0.6V, IRC32K off, RTC off, All GPIOs analog mode	4.5	—	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO=0.7V, IRC32K off, RTC off, All GPIOs analog mode	5.98	—	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO=0.8V, IRC32K off, RTC off, All GPIOs analog mode	7.97	—	mA
		V_{DD} = V_{DDA} = 3.3 V, LDO=0.9V, IRC32K off, RTC off, All GPIOs analog mode	10.86	—	mA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, FWDGT off, Backup SRAM off, RTC and LXTAL off	15.6	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT off, Backup SRAM on, RTC and LXTAL off	91.3	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT off, Backup SRAM off, RTC and LXTAL on	16.3	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT off, Backup SRAM on, RTC and LXTAL on	91.9	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT on, Backup SRAM off, RTC and LXTAL off	15.8	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT on, Backup SRAM on, RTC and LXTAL off	91.5	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT on, Backup SRAM off, RTC and LXTAL on	16.6	—	μA
		V_{DD} = V_{DDA} = 3.3 V, FWDGT on, Backup SRAM on, RTC and LXTAL on	92.2	—	μA
I_{BAT}	Battery supply current (Backup mode)	V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, Backup SRAM off, RTC and LXTAL off	3.9	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, Backup SRAM off, RTC and LXTAL off	1.1	—	μA

Symbol	Parameter	Conditions	Typ LDO regulator ON	Max	Unit
		V_{DD} off, V_{DDA} off, V_{BAT} = 3 V, Backup SRAM off, RTC and LXTAL off	0.3	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, Backup SRAM on, RTC and LXTAL off	79.4	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, Backup SRAM on, RTC and LXTAL off	77.1	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3 V, Backup SRAM on, RTC and LXTAL off	76.3	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, Backup SRAM off, RTC and LXTAL on	3.9	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, Backup SRAM off, RTC and LXTAL on	1.1	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3 V, Backup SRAM off, RTC and LXTAL on	0.3	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.6 V, Backup SRAM on, RTC and LXTAL on	79.5	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, Backup SRAM on, RTC and LXTAL on	77.1	—	μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3 V, Backup SRAM on, RTC and LXTAL on	76.2	—	μA

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Unless otherwise specified, all values given for T_J = 25 °C and test result is mean value.
(3) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTALor IRC32K are ON, an additional power consumption should be considered.
(4) During power consumption test, GPIO needs to be configure as Analog Input mode.

4.4. EMC characteristics

System level ESD (Electrostatic discharge, according to IEC 61000-4-2) and EFT (Electrical Fast Transient/burst, according to IEC 61000-4-4) testing result is given in the ***Table 4-9. System level ESD and EFT characteristics***[(1)]. System level ESD is for end-customer operation, it includes ESD field events on system level occur in an unprotected area (outside EPA). System level ESD protection necessary to satisfy higher ESD levels.

Table 4-9. System level ESD and EFT characteristics(1)

Symbol	Description	Conditions	Package	Class	Level
V_{ESD}	Contact / Air mode high voltage stressed on few special I/O pins	V_{DD} = 3.3 V, T_J = 25 °C, f_{HCLK} = 600 MHz IEC 61000-4-2	BGA176	CD 8kV AD 15kV	4A
			LQFP176	CD 4kV AD 8kV	2B
V_{EFT}	Fast transient high voltage burst stressed on Power and GND	V_{DD} = 3.3 V, T_J = 25 °C, f_{HCLK} = 600 MHz IEC 61000-4-4	BGA176	4kV	4A
			LQFP176	4kV	4A

(1) Value guaranteed by characterization, not 100% tested in production.

EMI (Electromagnetic Interference) emission test result is given in the ***Table 4-10. EMI characteristics***(1), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-10. EMI characteristics(1)

Symbol	Parameter	Conditions	Package	Mode	Max vs. [f_{HXTAL}/f_{HCLK}] 8/600 MHz				Unit
					0.1-30MHz	30-130MHz	130MHz-1GHz	1-3GHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_J = +25 °C, f_{HCLK} = 600 MHz, conforms to SAE J1752-3:2017	BGA176	LDO supply	2.55	7.55	6.17	6.70	dBμV
				SMPS supply	9.08	14.02	5.68	6.69	
				SMPS to LDO	7.06	13.30	8.05	6.66	
			LQFP176	LDO supply	4.00	7.36	12.64	6.86	
				SMPS supply	8.68	17.59	13.99	7.07	
				SMPS to LDO	8.72	17.14	13.36	7.21	

(1) Value guaranteed by characterization, not 100% tested in production.

Component level ESD include HBM (Human body model, according to ANSI/ESDA/JEDEC JS-001) and CDM (ANSI/ESDA/JEDEC JS-002), that ESD field events during manufacturing in an ESD protected area, such as PCB assembly/repair, IC assembly/test and Fab environment. The ESD protected area (EPA) has many measures, for instance ESD protective packaging, grounding person wrist strap to ground (or flooring/footwear), grounded work surface and ionizer.

Static latch-up (LU, according to JEDEC78) test is based on the two measurement methods, I/O current injection value (I-test) and power supply over-voltage value.

Table 4-11. Component level ESD characteristics(1)

Symbol	Description	Conditions	Package	Max	Unit	Level
V_{HBM}	Human body model electrostatic discharge voltage (Any pin combination)	T_J = 25 °C; JS-001-2017	BGA176	2000	V	2
V_{CDM}	Charge device model electrostatic discharge voltage (All pins)	T_J = 25 °C; JS-002-2018	BGA176	500	V	C2a
LU	I-test	T_A = 125 °C, JESD78F	BGA176	200	mA	Class II Level A
	V_{supply} over voltage			7.5	V	

(1) Value guaranteed by characterization, not 100% tested in production.

4.5. Power supply supervisor characteristics

Table 4-12. Power supply supervisor characteristics

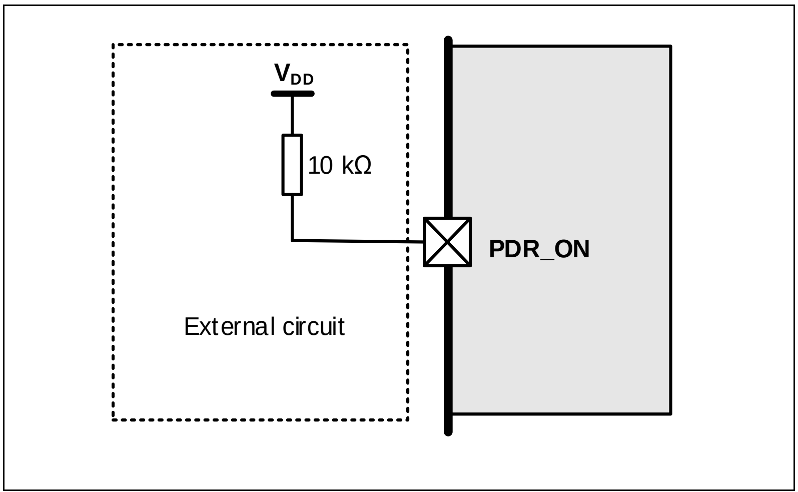
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LVD}(1)	Low voltage Detector level selection	LVDT<2:0> = 000(rising edge)	—	1.95	—	V
		LVDT<2:0> = 000(falling edge)	—	1.85	—	
		LVDT<2:0> = 001(rising edge)	—	2.10	—	
		LVDT<2:0> = 001(falling edge)	—	2.00	—	
		LVDT<2:0> = 010(rising edge)	—	2.25	—	
		LVDT<2:0> = 010(falling edge)	—	2.15	—	
		LVDT<2:0> = 011(rising edge)	—	2.40	—	
		LVDT<2:0> = 011(falling edge)	—	2.30	—	
		LVDT<2:0> = 100(rising edge)	—	2.56	—	
		LVDT<2:0> = 100(falling edge)	—	2.46	—	
		LVDT<2:0> = 101(rising edge)	—	2.70	—	
		LVDT<2:0> = 101(falling edge)	—	2.60	—	
		LVDT<2:0> = 110(rising edge)	—	2.86	—	
		LVDT<2:0> = 110(falling edge)	—	2.75	—	
$V_{LVDhyst}$(2)	LVD hysteris	—	—	100	—	mV
V_{POR}(1)	Power on reset threshold	—	—	1.53	—	V
V_{PDR}(1)	Power down reset	—	—	1.48	—	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	threshold					
$V_{PDRhyst}$(2)	PDR hysteresis	—	—	50	—	mV
V_{BOR3}(2)	Brownout level 3 threshold	Falling edge	—	2.6	—	V
		Rising edge	—	2.70	—	V
V_{BOR2}(2)	Brownout level 2 threshold	Falling edge	—	2.3	—	V
		Rising edge	—	2.4	—	V
V_{BOR1}(2)	Brownout level 1 threshold	Falling edge	—	2.0	—	V
		Rising edge	—	2.1	—	V
$V_{BORhyst}$(2)	BOR hysteresis	—	—	100	—	mV
$t_{RSTTEMPO}$(2)	Reset temporization	—	—	520	—	μs
V_{AVD_0}(1)	Analog voltage detector for V_{DDA} threshold 0	Rising edge	—	1.70	—	V
		Falling edge	—	1.60	—	
V_{AVD_1}(1)	Analog voltage detector for V_{DDA} threshold 1	Rising edge	—	2.10	—	
		Falling edge	—	2.00	—	
V_{AVD_2}(1)	Analog voltage detector for V_{DDA} threshold 2	Rising edge	—	2.49	—	
		Falling edge	—	2.40	—	
V_{AVD_3}(1)	Analog voltage detector for V_{DDA} threshold 3	Rising edge	—	2.79	—	
		Falling edge	—	2.70	—	
V_{hyst_AVD}(2)	Hysteresis of V_{DDA} voltage detector		—	100	—	mV

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

Figure 4-2. Recommended PDR_ON pin circuit(1)



(1) PDR_ON pin should be pulled up to V_{DD}.

4.6. Embedded USB regulator characteristics

Table 4-13. USB regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD50USB}$(1)	Supply voltage	—	4	5	5.5	V
$I_{DD50USB}$(2)	Current consumption	—	—	25	—	µA
$V_{REGOUT(V3.3V)}$ (1)	Regulated output voltage	—	3	—	3.6	V
I_{OUT}(2)	Output current load sinked by USB block	—	—	—	80	mA
T_{WKUP}(2)	V_{REGOUT} setting time	—	—	75	—	µs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

4.7. External clock characteristics

Table 4-14. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics(4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL}(1)	Crystal or ceramic frequency	1.71 V ≤ V_{DD} ≤ 3.6 V	4	25	50	MHz
R_F(2)	Feedback resistor	V_{DD} = 3.3 V	—	400	—	kΩ
C_{HXTAL}(2) (3)	Recommended matching capacitance on OSCIN and OSCOUT	—	—	20	30	pF
$Duty_{HXTAL}$(2)	Crystal or ceramic duty cycle	—	30	50	70	%
g_m(2)	Oscillator transconductance	Startup	—	27	—	mA/V
$I_{DD(HXTAL)}$ (1)	Crystal or ceramic operating current	HXTAL = 25 MHz	—	0.58	—	mA
$t_{ST(HXTAL)}$(1)	Crystal or ceramic startup time	HXTAL = 25 MHz	—	334	—	µs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.
(3) $C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.
(4) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-15. High speed external clock characteristics (HXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HXTAL_ext}(1)	External clock source or oscillator frequency	1.71 V ≤ V_{DD} ≤ 3.6 V	1	—	50	MHz
V_{HXTALH}(2)	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7 V_{DD}	—	V_{DD}	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HXTALL}(2)	OSCIN input pin low level voltage		V_{SS}	—	0.3 V_{DD}	V
$t_{H/L(HXTAL)}$ (2)	OSCIN high or low time	—	5	—	—	ns
$t_{R/F(HXTAL)}$ (2)	OSCIN rise or fall time	—	—	—	10	ns
$Duty_{HXTAL}$ (2)	Duty cycle	—	40	—	60	%

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-16. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics(5)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL}(1)	Crystal or ceramic frequency	—	—	32.768	—	kHz
C_{LXTAL}(2) (3)	Recommended matching capacitance on OSC32IN and OSC32OUT	—	—	15	—	pF
$Duty_{LXTAL}$(2)	Crystal or ceramic duty cycle	—	30	—	70	%
g_m(2)	Oscillator transconductance	LXTALDRI[1:0] = 00	—	4.88	—	μA/V
		LXTALDRI[1:0] = 01	—	7.32	—	
		LXTALDRI[1:0] = 10	—	14.61	—	
		LXTALDRI[1:0] = 11	—	21.94	—	
$I_{DD(LXTAL)}$(1)	Crystal or ceramic operating current	LXTALDRI[1:0] = 00	—	480	—	nA
		LXTALDRI[1:0] = 01	—	590	—	
		LXTALDRI[1:0] = 10	—	900	—	
		LXTALDRI[1:0] = 11	—	1210	—	
$t_{ST(LXTAL)}$(1)(4)	Crystal or ceramic startup time	LXTALDRI[1:0] = 00	—	453.9	—	ms
		LXTALDRI[1:0] = 01	—	322.7	—	
		LXTALDRI[1:0] = 10	—	220.4	—	
		LXTALDRI[1:0] = 11	—	192.4	—	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.
(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.
(4) $t_{ST(LXTAL)}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is set. This value varies significantly with the crystal manufacturer.
(5) More details about g_m could be found in ***AN052 GD32 MCU Resonator-Based Clock Circuits.***

Table 4-17. Low speed external user clock characteristics (LXTAL in bypass mode)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LXTAL_ext}(1)	External clock source or oscillator frequency	V_{DD} = 3.3 V	—	32.768	1000	kHz
V_{LXTALH}(2)	OSC32IN input pin high level voltage	—	0.7 V_{DD}	—	V_{DD}	V
V_{LXTALL}(2)	OSC32IN input pin low level voltage	—	V_{SS}	—	0.3 V_{DD}	
$t_{H/L(LXTAL)}$ (2)	OSC32IN high or low time	—	450	—	—	ns
$t_{R/F(LXTAL)}$ (2)	OSC32IN rise or fall time	—	—	—	50	
$Duty_{LXTAL}$	Duty cycle	—	30	50	70	%

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

Figure 4-3. Recommended external OSCIN and OSCOUT pins circuit for crystal

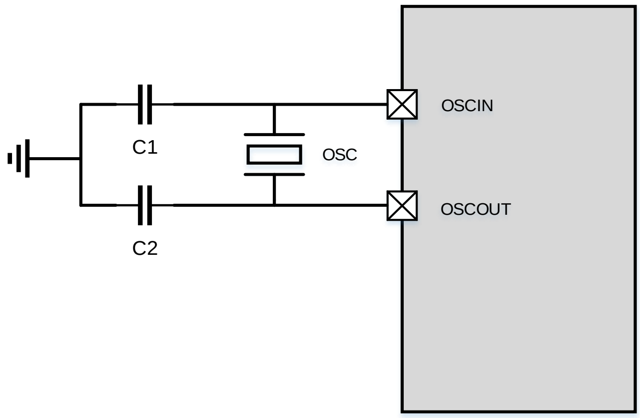
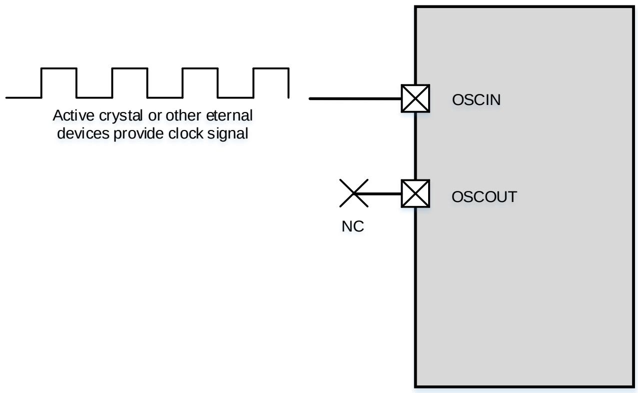


Figure 4-4. Recommended external OSCIN and OSCOUT pins circuit for oscillator



4.8. Internal clock characteristics

Table 4-18. High speed internal clock (IRC48M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = 3.3 V	—	48	—	MHz
$Drift_{IRC48M}$	IRC48M oscillator Frequency Drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_J = -40 °C ~ +85 °C(1)	—	-0.64 ~ +0.55	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_J = 25 °C	47.5	—	48.5	MHz
	IRC48M oscillator Frequency accuracy, User trimming step(1)	—	—	0.7	—	%
$Duty_{IRC48M}$(2)	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC48M)}$(1)	IRC48M oscillator operating current	—	—	330	—	μA
$t_{ST(IRC48M)}$(1)	IRC48M oscillator startup time	—	—	2.85	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-19. High speed internal clock (IRC64M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC64M}	High Speed Internal Oscillator (IRC64M) frequency	V_{DD} = 3.3 V	—	64	—	MHz
$Drift_{IRC64M}$	IRC64M oscillator Frequency drift, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_J = -40 °C ~ +85 °C(1)	—	-0.19 ~ +0.85	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_J = 25 °C	63.68	—	64.32	MHz
	IRC64M oscillator Frequency accuracy, User trimming step(1)	—	—	0.23	—	%
$Duty_{IRC64M}$(2)	IRC64M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDA(IRC64M)}$(1)	IRC64M oscillator operating current	—	—	500	—	μA
$t_{ST(IRC64M)}$(1)	IRC64M oscillator startup time	—	—	1.95	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-20. Low power internal clock (LPIRC4M) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{LPIRC4M}$	High Speed Internal Oscillator (LPIRC4M) frequency	V_{DD} = 3.3 V	—	4	—	MHz
$ACC_{LPIRC4M}$	LPIRC4M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_J = -40 °C ~ +85 °C(1)	—	-0.96 ~ +1.02	—	%
		V_{DD} = V_{DDA} = 3.3 V, T_J = 25 °C	3.96	—	4.04	MHz
	LPIRC4M oscillator Frequency accuracy, User trimming step(1)	—	—	0.4	—	%
$D_{LPIRC4M}$(2)	LPIRC4M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDALPIRC4M}$(1)	LPIRC4M oscillator operating current	—	—	30	—	μA
$t_{SULPIRC4M}$(1)	LPIRC4M oscillator startup time	—	—	1.64	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-21. Low speed internal clock (IRC32K) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{IRC32K}(1)	Low Speed Internal oscillator (IRC32K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_J = -40 °C ~ +85 °C	—	32	—	kHz
$t_{SUIRC32K}$(2)	IRC32K oscillator startup time	—	—	50.72	—	μs

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

4.9. PLL characteristics

Table 4-22. PLL0/1/2 characteristics (wide VCO frequency range)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	2	—	16	MHz
	PLL input clock duty cycle	—	10	—	90	%
f_{VCO}(1)	PLL VCO output clock frequency	—	100	—	850	MHz
t_{LOCK}(2)	PLL lock time	—	—	200	500	μs
I_{DD}(2)	Current consumption on V_{DD}	VCO freq = 800 MHz	—	1.5	—	mA
		VCO freq = 100 MHz	—	0.3	—	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Jitter_{PLL}$(2)	Cycle to cycle Jitter(rms)	f_{PLL_OUT} = f_{VCO_OUT}/10	f_{VCO_OUT} = 100 MHz	—	100	—	ps
			f_{VCO_OUT} = 400 MHz	—	19	—	
			f_{VCO_OUT} = 800 MHz	—	16	—	
	Period jitter(rms)		f_{VCO_OUT} = 100 MHz	—	80	—	
			f_{VCO_OUT} = 400 MHz	—	12	—	
			f_{VCO_OUT} = 800 MHz	—	10	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-23. PLL0/1/2 characteristics (narrow VCO frequency range)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—		1	—	2	MHz
	PLL input clock duty cycle	—		10	—	90	%
f_{VCO}(1)	PLL VCO output clock frequency	—		100	—	500	MHz
t_{LOCK}(2)	PLL lock time	—		—	200	500	μs
I_{PLL}(2)	Current consumption on V_{DD}	VCO freq = 500 MHz		—	1.2	—	mA
$Jitter_{PLL}$(2)	Cycle to cycle Jitter(rms)	f_{PLL_OUT} = f_{VCO_OUT}/10	f_{VCO_OUT} = 500 MHz	—	16	—	±ps
			f_{VCO_OUT} = 500 MHz	—	10	—	

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

Table 4-24. PLLUSBHS0/1 characteristics(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}(1)	PLL input clock frequency	—	4	—	30	MHz
f_{PLLOUT}(1)	PLL output clock frequency	—	—	480	—	MHz
f_{VCO}(1)	PLL VCO output clock frequency	—	—	480	—	MHz
t_{LOCK}(1)	PLL lock time	—	—	100	150	μs
I_{DDA}(2)	Current consumption on V_{DDA}	—	—	1.7	—	mA
$Jitter_{PLL}$	Cycle to cycle Jitter(rms)	System clock	—	40	—	ps
	Cycle to cycle Jitter（peak to peak）		—	400	—	

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.
(3) Value given with main PLL running.

4.10. Memory characteristics

Table 4-25. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ(1)	Max(2)	Unit
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	—	100	—	—	kcycles
t_{RET}	Data retention time	—	—	20	—	years
t_{PROG}	Word programming time	T_A = -40°C ~ +105 °C	—	1	—	ms
$t_{ERASE4kB}$	Sector(4kB) erase time	T_A = -40°C ~ +105 °C	—	100	—	ms
$t_{MERASE(1MB)}$	Mass erase time	T_A = -40°C ~ +105 °C	—	8	—	s
$t_{MERASE(2MB)}$	Mass erase time	T_A = -40°C ~ +105 °C	—	16	—	s
$t_{MERASE(3840kB)}$	Mass erase time	T_A = -40°C ~ +105 °C	—	30	—	s

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

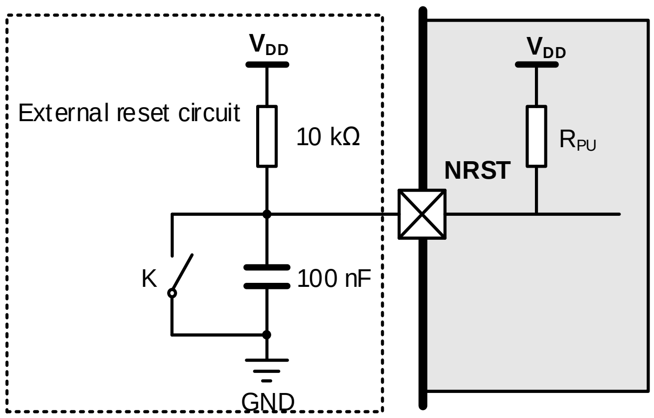
4.11. NRST pin characteristics

Table 4-26. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(2)	NRST Input low level voltage	$V_{DD} = V_{DDA}$ = 1.71 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(2)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	300	—	mV
$V_{IL(NRST)}$(2)	NRST Input low level voltage	$V_{DD} = V_{DDA}$ = 3.3 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(2)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	310	—	mV
$V_{IL(NRST)}$(2)	NRST Input low level voltage	$V_{DD} = V_{DDA}$ = 3.6 V	-0.3	—	0.3 V_{DD}	V
$V_{IH(NRST)}$(2)	NRST Input high level voltage		0.7 V_{DD}	—	V_{DD} + 0.3	
V_{hyst}(1)	Schmidt trigger Voltage hysteresis		—	320	—	mV
R_{pu}(2)	Pull-up equivalent resistor	—	—	40	—	kΩ

(1) Value guaranteed by characterization, not 100% tested in production.
(2) Value guaranteed by design, not 100% tested in production.

Figure 4-5. Recommended external NRST pin circuit



4.12. GPIO characteristics

Table 4-27. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low level voltage	1.71 V < V_{DD} < 3.6 V	—	—	0.3V_{DD}	V
V_{IH}(1)	I/O input high level voltage	1.71 V <V_{DD} < 3.6 V	0.7V_{DD}	—	—	V
V_{HYS}(1)	input hysteresis	V_{DD} =3.3 V	—	360	—	mV
I_{leak}	Input leakage current	0 < V_{IN} ≤ V_{DD}	—	—	±2	μA
R_{PU}(1)	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	—	40	—	kΩ
R_{PD}(1)	Weak pull-down equivalent resistor	V_{IN} = V_{DD}	—	40	—	kΩ

(1) Value guaranteed by design, not 100% tested in production.

Table 4-28. Output voltage characteristics for all I/Os except PC13, PC14, PC15(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL} (IO_speed=max)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	0.094	—	V
		V_{DD} = 3.3 V	—	0.058	—	
		V_{DD} = 3.6 V	—	0.057	—	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	0.253	—	
		V_{DD} = 3.3 V	—	0.15	—	
		V_{DD} = 3.6 V	—	0.147	—	
V_{OH} (IO_speed=max)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	1.6	—	
		V_{DD} = 3.3 V	—	3.226	—	
		V_{DD} = 3.6 V	—	3.529	—	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	1.423	—	
		V_{DD} = 3.3 V	—	3.114	—	
		V_{DD} = 3.6 V	—	3.416	—	
V_{OL}	Low level output	V_{DD} = 1.71 V	—	0.139	—	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
(IO_speed=85MHz)	voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 3.3 V	—	0.083	—	
		V_{DD} = 3.6 V	—	0.08	—	
	Low level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	0.404	—	
		V_{DD} = 3.3 V	—	0.209	—	
		V_{DD} = 3.6 V	—	0.204	—	
V_{OH} (IO_speed=85MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	1.547	—	
		V_{DD} = 3.3 V	—	3.197	—	
		V_{DD} = 3.6 V	—	3.5	—	
	High level output voltage for an IO Pin (I_{IO} = +20 mA)	V_{DD} = 1.71 V	—	1.254	—	
		V_{DD} = 3.3 V	—	3.037	—	
		V_{DD} = 3.6 V	—	3.342	—	
V_{OL} (IO_speed=60MHz)	Low level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	0.162	—	V
		V_{DD} = 3.3 V	—	0.092	—	
		V_{DD} = 3.6 V	—	0.091	—	
	Low level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 1.71 V	—	0.359	—	
		V_{DD} = 3.3 V	—	0.188	—	
		V_{DD} = 3.6 V	—	0.184	—	
V_{OH} (IO_speed=60MHz)	High level output voltage for an IO Pin (I_{IO} = +8 mA)	V_{DD} = 1.71 V	—	1.523	—	
		V_{DD} = 3.3 V	—	3.181	—	
		V_{DD} = 3.6 V	—	3.484	—	
	High level output voltage for an IO Pin (I_{IO} = +16 mA)	V_{DD} = 1.71 V	—	1.298	—	
		V_{DD} = 3.3 V	—	3.060	—	
		V_{DD} = 3.6 V	—	3.367	—	
V_{OL} (IO_speed=12MHz)	Low level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.71 V	—	0.052	—	V
		V_{DD} = 3.3 V	—	0.029	—	
		V_{DD} = 3.6 V	—	0.028	—	
	Low level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	—	0.235	—	
		V_{DD} = 3.3 V	—	0.119	—	
		V_{DD} = 3.6 V	—	0.116	—	
V_{OH} (IO_speed=12MHz)	High level output voltage for an IO Pin (I_{IO} = +1 mA)	V_{DD} = 1.71 V	—	1.647	—	V
		V_{DD} = 3.3 V	—	3.26	—	
		V_{DD} = 3.6 V	—	3.562	—	
	High level output voltage for an IO Pin (I_{IO} = +4 mA)	V_{DD} = 1.71 V	—	1.437	—	
		V_{DD} = 3.3 V	—	3.142	—	
		V_{DD} = 3.6 V	—	3.451	—	

(1) Value guaranteed by characterization, not 100% tested in production.

(2) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current.

Table 4-29. Output timing characteristics (IOSPDOP OFF) (3)(4)

Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	tr/tf(2)	Output high to low level fall time and	2.5 V ≤ VDD ≤ 3.6 V, C_L = 50 pF	—	7.66	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	17.38	—	

Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		output low to high level rise time	2.5 V ≤ VDD ≤ 3.6 V, C_L = 30 pF	—	3.98	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	13.72	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 10 pF	—	2.79	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	9.33	—	
01	tr/tf(2)	Output high to low level fall time and output low to high level rise time	2.5 V ≤ VDD ≤ 3.6 V, C_L = 50 pF	—	3.6	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	4.5	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 30 pF	—	2.6	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	3.38	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 10 pF	—	1.64	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	2.43	—	
10	tr/tf(2)	Output high to low level fall time and output low to high level rise time	2.5 V ≤ VDD ≤ 3.6 V, C_L = 50 pF	—	3.3	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	3.5	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 30 pF	—	2.5	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.6	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 10 pF	—	1.5	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	1.7	—	
11	tr/tf(2)	Output high to low level fall time and output low to high level rise time	2.5 V ≤ VDD ≤ 3.6 V, C_L = 50 pF	—	3.3	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	3.5	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 30 pF	—	2.5	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.6	—	
			2.5 V ≤ VDD ≤ 3.6 V, C_L = 10 pF	—	1.5	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	1.7	—	

(1) The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3 T Skew ≤ 1/20 T 45% < Duty cycle < 55%

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by characterization, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

Table 4-30. Output timing characteristics (IOSPDOP ON) (1)(3)(4)

Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	16.5	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	11.1	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	8.1	—	
01	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	4	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.9	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	2	—	
10	tr/tf(2)	Output high to low level fall time and output low to high level rise time	1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	3.8	—	ns
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.8	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	1.8	—	
11	tr/tf(2)	Output high to low	1.71 V ≤ VDD ≤ 2.5 V, C_L = 50 pF	—	3.5	—	ns

Speed	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		level fall time and output low to high level rise time	1.71 V ≤ VDD ≤ 2.5 V, C_L = 30 pF	—	2.6	—	
			1.71 V ≤ VDD ≤ 2.5 V, C_L = 10 pF	—	1.6	—	

(1) The maximum frequency is defined with the following conditions: (tr+tf) ≤ 2/3 T Skew ≤ 1/20 T 45% < Duty cycle < 55%

(2) The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.

(3) Value guaranteed by characterization, not 100% tested in production.

(4) The data is for reference only, and the specific values are related to PCB Layout.

4.13. 14-bit ADC characteristics

Table 4-31. 14-bit ADC characteristics

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—				1.8	—	3.6	V
V_{REFP}(2)	Positive Reference Voltage	V_{DDA} ≥ 2.4 V				2.4	—	V_{DDA}	V
		V_{DDA} < 2.4 V				1.8	—	V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage	—				V_{SSA}			V
f_{ADC}(1)	ADC clock	2.7 V ≤ V_{DDA} ≤ 3.6 V 2.7 V ≤ V_{REFP} ≤ V_{DDA}				0.1	—	72	MHz
		2.4 V ≤ V_{DDA} ≤ 2.7 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}				0.1	—	54	MHz
		1.8 V ≤ V_{DDA} ≤ 2.4 V 1.8 V ≤ V_{REFP} ≤ V_{DDA}				0.1	—	36	MHz
f_S(1)	Sampling rate	Resolution = 14 bits	2.7 V ≤ V_{DDA} ≤ 3.6 V 2.7 V ≤ V_{REFP} ≤V_{DDA}	f_{ADC} = 72 MHz	SMP = 3.5	—	—	4	MSPS
			2.4 V ≤ V_{DDA} ≤ 2.7 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 54 MHz	SMP = 3.5	—	—	3	
			1.8 V ≤ V_{DDA} ≤ 2.4 V 1.8 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 36 MHz	SMP = 3.5	—	—	2	
		Resolution = 12 bits	2.7 V ≤ V_{DDA} ≤ 3.6 V 2.7 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 72 MHz	SMP = 3.5	—	—	4.5	
			2.4 V ≤ V_{DDA} ≤ 2.7 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 54 MHz	SMP = 3.5	—	—	3.37	
			1.8 V ≤ V_{DDA} ≤ 2.4 V 1.8 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 36 MHz	SMP = 3.5	—	—	2.25	
		Resolution = 10 bits	2.7 V ≤ V_{DDA} ≤ 3.6 V 2.7 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 72 MHz	SMP = 3.5	—	—	5.14	
			2.4 V ≤ V_{DDA} ≤ 2.7 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 54 MHz	SMP = 3.5	—	—	3.85	
			1.8 V ≤ V_{DDA} ≤ 2.4 V 1.8 V ≤ V_{REFP} ≤ V_{DDA}	f_{ADC} = 36 MHz	SMP = 3.5	—	—	2.57	

Symbol	Parameter	Conditions				Min	Typ	Max	Unit
		Resolution = 8 bits	$2.7\ V \le V_{DDA} \le 3.6\ V$ $2.7\ V \le V_{REFP} \le V_{DDA}$	f_{ADC} = 72 MHz	SMP = 3.5	—	—	6	
			$2.4\ V \le V_{DDA} \le 2.7\ V$ $2.4\ V \le V_{REFP} \le V_{DDA}$	f_{ADC} = 54 MHz	SMP = 3.5	—	—	4.5	
			$1.8\ V \le V_{DDA} \le 2.4\ V$ $1.8\ V \le V_{REFP} \le V_{DDA}$	f_{ADC} = 36 MHz	SMP = 3.5	—	—	3	
t_{TRIG}(1)	External trigger period	Resolution = 14 bits				—	—	18	1/ f_{ADC}
V_{AIN}(1)	Conversion voltage range	—				0	—	V_{REFP}	V
V_{CMIV}(1)	Common mode input voltage	—				V_{REFP}/2-10%	V_{REFP}/2	V_{REFP}/2+10%	V
R_{AIN}(1)	External input impedance	Resolution = 14 bits				—	—	84.4	kΩ
		Resolution = 12 bits				—	—	96.5	
		Resolution = 10 bits				—	—	112	
		Resolution = 8 bits				—	—	135	
R_{ADC}(1)	Internal resistance					—	150	—	Ω
C_{ADC}(1)	Input sampling capacitance	—				—	12	—	pF
t_{STAB}	ADC Power-up time	—				1	—	—	μs
t_{CAL}(1)	Offset and linearity calibration time	—				TBD			1/f_{ADC}
t_{OFF_CAL}(1)	Offset calibration time	—				TBD			1/f_{ADC}
t_s(1)	Sampling time	—				3.5	—	810.5	1/f_{ADC}
t_{CONV}(1)	Total conversion time (including sampling time)	Resolution = N bits				N+4	—	—	1/f_{ADC}

(1) Value guaranteed by design, not 100% tested in production.

(2) Depending on the package, V_{REFP} can be internally connected to V_{DDA} and V_{REFN} to V_{SSA}.

***Equation 1**:* R_{AIN} max formula $R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$

The formula above ***Equation 1*** is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 14 (from 14-bit resolution).

Table 4-32. ADC R_{AIN} max for f_{ADC} = 72 MHz (14-bit ADC) (1)(2)

Resolution	Sampling cycles @ 72 MHz	R_{AIN} max (kΩ)
14 bits	3.5	0.21
	6.5	0.52
	12.5	1.15

Resolution	Sampling cycles @ 72 MHz	R_{AIN} max (kΩ)
	24.5	2.40
	47.5	4.80
	92.5	9.50
	247.5	25.6
	810.5	84.4
12 bits	3.5	0.26
	6.5	0.62
	12.5	1.34
	24.5	2.77
	47.5	5.51
	92.5	10.8
	247.5	29.3
	810.5	96.5
10 bits	3.5	0.33
	6.5	0.75
	12.5	1.58
	24.5	3.25
	47.5	6.45
	92.5	12.7
	247.5	34.2
	810.5	112
8 bits	3.5	0.43
	6.5	0.93
	12.5	1.93
	24.5	3.94
	47.5	7.78
	92.5	15.2
	247.5	41.1
	810.5	135

(1) Value guaranteed by design, not 100% tested in production.

(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-33. 14-bit ADC accuracy(1)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	Single ended	TBD	TBD	LSB
		Differential	TBD	TBD	
EO	Offset error	Single ended	TBD	TBD	
		Differential	TBD	TBD	
EG	Gain error	Single ended	TBD	TBD	
		Differential	TBD	TBD	

DNL	Differential linearity error	Single ended	TBD	TBD	
		Differential	TBD	TBD	
INL	Integral linearity error	Single ended	TBD	TBD	
		Differential	TBD	TBD	
ENOB	Effective number of bits	Single ended	TBD	—	Bits
		Differential	TBD	—	
SNDR	Signal-to-noise and distortion ratio	Single ended	TBD	—	
		Differential	TBD	—	
SNR	Signal-to-noise ratio	Single ended	TBD	—	dB
		Differential	TBD	—	
THD	Total harmonic distortion	Single ended	TBD	—	
		Differential	TBD	—	

(1) Guaranteed by characterization results for BGA packages. The values for LQFP packages might differ.

4.14. 12-bit ADC characteristics

Table 4-34. 12-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Operating voltage	—	1.71	—	3.6	V
V_{REFP}(2)	Positive Reference Voltage	$V_{DDA} \geq V_{REFP}$	1.71	—	V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage	—	V_{SSA}			V
f_{ADC}(1)	ADC clock	$1.71\ V \leq V_{DDA} \leq 3.6\ V$ $2.4\ V \leq V_{REFP} \leq V_{DDA}$	0.1	—	80	MHz
		$1.71\ V \leq V_{DDA} \leq 2.4\ V$ $1.71\ V \leq V_{REFP} \leq V_{DDA}$	0.1	—	60	MHz
f_S(1)	—	Resolution = 12 bits, $2.4\ V \leq V_{DDA} \leq 3.6\ V$, $2.4\ V \leq V_{REFP} \leq V_{DDA}$, $-40\ °C \leq T_J \leq 125\ °C$, f_{ADC} = 80 MHz, SMP = 2.5	—	—	5.3	MSPS
		Resolution = 12 bits, $1.71\ V \leq V_{DDA} \leq 2.4\ V$, $1.71\ V \leq V_{REFP} \leq V_{DDA}$, $-40\ °C \leq T_J \leq 125\ °C$, f_{ADC} = 60 MHz, SMP = 2.5	—	—	4	

Symbol	Parameter	Conditions					Min	Typ	Max	Unit
		Resolution = 10 bits	2.4 V≤V_{DDA}≤3.6 V 2.4 V≤V_{REFP}≤V_{DDA}	–40 °C ≤ T_J ≤ 125 °C	f_{ADC} = 80 MHz	SMP = 2.5	—	—	6.1	
			1.71 V ≤ V_{DDA} ≤ 2.4 V 1.71 V ≤ V_{REFP} ≤ V_{DDA}		f_{ADC} = 60 MHz		—	—	4.6	
		Resolution = 8 bits	2.4 V ≤ V_{DDA} ≤ 3.6 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	–40 °C ≤ T_J ≤ 125 °C	f_{ADC} = 80 MHz	SMP = 2.5	—	—	7.2	
			1.71 V ≤ V_{DDA} ≤ 2.4 V 1.71 V ≤ V_{REFP} ≤ V_{DDA}		f_{ADC} = 60 MHz		—	—	5.4	
		Resolution = 6 bits	2.4 V ≤ V_{DDA} ≤ 3.6 V 2.4 V ≤ V_{REFP} ≤ V_{DDA}	–40 °C ≤ T_J ≤ 125 °C	f_{ADC} = 80 MHz	SMP = 2.5	—	—	8.8	
			1.71 V ≤ V_{DDA} ≤ 2.4 V 1.71 V ≤ V_{REFP} ≤ V_{DDA}		f_{ADC} = 60 MHz		—	—	6.6	
t_{TRIG}(1)	External trigger period	Resolution = 12 bits					—	—	15	1/f_{ADC}
V_{AIN}	Conversion voltage range	—					0	—	V_{REFP}	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CMIV}	Common mode input voltage	—	V_{REFP}/2-10%	V_{REFP}/2	V_{REFP}/2-10%	
R_{AIN}	External input impedance	Resolution = 12 bits	—	—	109	kΩ
		Resolution = 10 bits	—	—	128	
		Resolution = 8 bits	—	—	153	
		Resolution = 6 bits	—	—	192	
R_{ADC}	Internal resistance	—	—	250	—	Ω
C_{ADC}	Input capacitance	—	—	7.5	—	pF
t_{STAB}	ADC Power-up time	—	-	1	—	μs
t_{OFF_CAL}	Offset calibration time	—	46	—	—	1/f_{ADC}
t_s	Sampling time	—	2.5	—	640.5	1/f_{ADC}
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits	3+N	—	—	1/ f_{ADC}

(1) Value guaranteed by design, not 100% tested in production.
(2) Depending on the package, V_{REFP} can be internally connected to V_{DDA} and V_{REFN} to V_{SSA}.
(3) Value guaranteed by characterization, not 100% tested in production.

Table 4-35. ADC R_{AIN} max for f_{ADC} = 80 MHz (12-bit ADC) (1)(2)

Resolution	Sampling cycles @ 80 MHz	R_{AIN} max (kΩ)
12 bits	2.5	0.17
	6.5	0.86
	12.5	1.89
	24.5	3.95
	47.5	7.90
	92.5	15.6
	247.5	42.2
	640.5	109
10 bits	2.5	0.25
	6.5	1.05
	12.5	2.25
	24.5	4.65

Resolution	Sampling cycles @ 80 MHz	R_{AIN} max (kΩ)
	47.5	9.26
	92.5	18.2
	247.5	49.3
	640.5	128
8 bits	2.5	0.35
	6.5	1.31
	12.5	2.75
	24.5	5.64
	47.5	11.1
	92.5	21.9
	247.5	59.2
	640.5	153
6 bits	2.5	0.50
	6.5	1.70
	12.5	3.50
	24.5	7.11
	47.5	14.0
	92.5	27.5
	247.5	74.1
	640.5	192

(1) Value guaranteed by design, not 100% tested in production.
(2) The R_{AIN} value was calculated by theory and stray capacitance of actual pcb has not been taken into account.

Table 4-36. ADC dynamic accuracy at f_{ADC} = 60 MHz V_{REFP} = 1.8 V(1)(2)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 60 MHz V_{REFP} = 1.8 V Input Frequency = 20 kHz	Single ended	—	10.9	—	bits
			Differential	—	11.4	—	
SNDR	Signal-to-noise and distortion ratio		Single ended	—	67.5	—	dB
			Differential	—	70.7	—	
SNR	Signal-to-noise ratio		Single ended	—	67.6	—	
			Differential	—	70.8	—	
THD	Total harmonic distortion		Single ended	—	-83.1	—	
			Differential	—	-86.6	—	

(1) Guaranteed by characterization results for BGA packages. The values for LQFP packages might differ.
(2) The test was carried out under the LDO power supply mode.

Table 4-37. ADC dynamic accuracy at f_{ADC} = 80 MHz V_{REFP} = 2.4 V(1)(2)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 80 MHz V_{REFP} = 2.4 V Input Frequency = 20 kHz	Single ended	—	11.1	—	bits
			Differential	—	11.6	—	
SNDR	Signal-to-noise and distortion ratio		Single ended	—	68.7	—	dB
			Differential	—	71.6	—	

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
SNR	Signal-to-noise ratio		Single ended	—	68.8	—	
			Differential	—	71.7	—	
THD	Total harmonic distortion		Single ended	—	-83.6	—	
			Differential	—	-86.8	—	

(1) Guaranteed by characterization results for BGA packages. The values for LQFP packages might differ.

(2) The test was carried out under the LDO power supply mode.

Table 4-38. ADC dynamic accuracy at f_{ADC} = 80 MHz V_{REFP} = 3.3 V(1)(2)

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 80 MHz V_{REFP} = 3.3 V Input Frequency = 20 kHz	Single ended	—	11.1	—	bits
			Differential	—	11.5	—	
SNDR	Signal-to-noise and distortion ratio		Single ended	—	68.5	—	dB
			Differential	—	71.5	—	
SNR	Signal-to-noise ratio		Single ended	—	68.6	—	
			Differential	—	71.6	—	
THD	Total harmonic distortion		Single ended	—	-83.3	—	
			Differential	—	-85.9	—	

(1) Guaranteed by characterization results for BGA packages. The values for LQFP packages might differ.

(2) The test was carried out under the LDO power supply mode.

Table 4-39. ADC static accuracy at f_{ADC} = 60 MHz V_{REFP} = 1.8 V(1)(2)

Symbol	Parameter	Test conditions		Typ	Max	Unit
EO	Offset error	f_{ADC} = 60 MHz V_{REFP} = 1.8 V Input Frequency = 1 kHz	Single ended	±1.5	—	LSB
			Differential	±0.5	—	
DNL	Differential linearity error		Single ended	+1.1 / -1	—	
			Differential	±0.9	—	
INL	Integral linearity error		Single ended	±0.8	—	
			Differential	±1	—	

(1) Guaranteed by characterization results for BGA packages. The values for LQFP packages might differ.

(2) The test was carried out under the LDO power supply mode.

Table 4-40. ADC static accuracy at f_{ADC} = 80 MHz V_{REFP} = 2.4 V(1)(2)

Symbol	Parameter	Test conditions		Typ	Max	Unit
EO	Offset error	f_{ADC} = 80 MHz V_{REFP} = 2.4 V Input Frequency = 1 kHz	Single ended	±1	—	LSB
			Differential	±0.5	—	
DNL	Differential linearity error		Single ended	±0.7	—	
			Differential	±0.5	—	
INL	Integral linearity error		Single ended	±1.2	—	
			Differential	±1.2	—	

(1) Guaranteed by characterization results for BGA packages. The values for LQFP packages might differ.

(2) The test was carried out under the LDO power supply mode.

Table 4-41. ADC static accuracy at f_{ADC} = 80 MHz V_{REFP} = 3.3 V(1)(2)

Symbol	Parameter	Test conditions		Typ	Max	Unit
EO	Offset error	f_{ADC} = 80 MHz	Single ended	±1	—	LSB

		V_{REFP} = 3.3 V Input Frequency = 1 kHz	Differential	±0.5	—	
DNL	Differential linearity error		Single ended	±0.5	—	
			Differential	±0.5	—	
INL	Integral linearity error		Single ended	±1.5	—	
			Differential	±0.9	—	

(1) Guaranteed by characterization results for BGA packages. The values for LQFP packages might differ.

(2) The test was carried out under the LDO power supply mode.

4.15. High-precision temperature sensor characteristics

Table 4-42. High-precision temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{25}[1]	Uncalibrated Offset	T_J = 25°C	—	1005.62	—	mV
E_{OFF}[1]	Uncalibrated Offset Error	T_J = 25°C	—	1.5	—	mV
Avg_Slope[1]	Average slope	—	—	3.3	—	mV/°C
E_M[1]	Slope Error	—	—	30	—	μV/°C
LIN[2]	Linearity	T_J = -40 °C to 125 °C	—	1.5	—	°C
t_{s_temp}	ADC sampling time when reading the temperature	—	10	—	—	μs
t_{ON}[1]	Turn-on Time	f_{ADC} = 5 MHz, t_{s_temp} = 10 μs	—	37.8	—	μs
ETOT[1][3]	Temp Sensor Error Using Typical Slope and Factory-Calibrated Offset	T_J = -40 °C to 125 °C	—	-2~4	—	°C

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

(3) The error is the average result of 100 times and represents the chip junction temperature error. The chip self-heating shall be considered when testing ambient temperature

Table 4-43. High-precision temperature sensor calibration values

Symbol	Parameter	Memory address
HPTS_CAL	High-precision temperature sensor raw data acquired value at 25°C,V_{REFP} = 3.3 V	0x1FF0F7C4

4.16. Temperature sensor characteristics

Table 4-44. Temperature sensor characteristics[1]

Symbol	Parameter	Min	Typ	Max	Unit
T_L	V_{SENSE} linearity with temperature	—	±3.5	—	°C
Avg_Slope	Average slope	—	1.84	—	mV/°C
V_{25}	Voltage at T_J = 25 °C	—	0.66	—	V
t_{s_temp}[2]	ADC sampling time when reading the temperature	—	17.1	—	μs

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

Table 4-45. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 25 °C, V_{REFP} = 3.3 V	0x1FF0F7C0
TS_CAL2	Temperature sensor raw data acquired value at -40 °C, V_{REFP} = 3.3 V	0x1FF0F7C2

4.17. Low power digital temperature sensor characteristics

Table 4-46. Low power digital temperature sensor characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(2)	Supply voltage	—	1.71	3.3	3.6	V
f_{DTS}(1)	Output Clock frequency	—	626	798	1030	kHz
T_{LC}(1)	Temperature linearity coefficient	—	1307	2340	2744	Hz/°C
$T_{TOTAL(ERROR)}$(1)	Temperature offset measurement	T_J = -40 °C to 25 °C	-6.4	—	2.4	°C
		T_J = 25 °C to $T_J$max	-10.6	—	1.3	
t_{WAKE_UP}(2)	Wake-up time from off state until DTS ready bit is set	—	—	352	—	μs
I_{LPDTS}(1)	LPDTS consumption	—	—	26	—	μA

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

4.18. Voltage reference buffer characteristics

Table 4-47. Voltage reference buffer characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Supply voltage	Normal mode, V_{DDA} = 3.3V	VREFS = 00	2.8	3.3	3.6	V
			VREFS = 01	2.4	—	3.6	
			VREFS = 10	2.1	—	3.6	
			VREFS = 11	1.8	—	3.6	
		Degraded mode	VREFS = 00	1.71	—	2.8	
			VREFS = 01	1.71	—	2.4	
			VREFS = 10	1.71	—	2.1	
			VREFS = 11	1.71	—	1.8	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	Normal mode, at 3.3 V, -40 ~	VREFS = 00	2.493	2.5	2.507	
			VREFS = 01	2.052	2.0585	2.065	
			VREFS = 10	1.801	1.8072	1.814	
			VREFS = 11	1.502	1.5065	1.512	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		85 °C(2)					
		Degraded mode	VREFS = 00	V_{DDA}-50mV	—	V_{DDA}	
			VREFS = 01	V_{DDA}-50mV	—	V_{DDA}	
			VREFS = 10	V_{DDA}-50mV	—	V_{DDA}	
			VREFS = 11	V_{DDA}-210mV	—	V_{DDA}	
TRIM	Trim step resolution	—		—	0.14	0.152	%
C_L	Load capacitor	—		0.5	1	1.5	µF
ESR	Equivalent Serial Resistor of CL	—		—	—	2	Ω
I_{LOAD}	Load current	—		—	—	4	mA
t_{START}	Start-up time	C_L = 0.5 µF	—	—	546	—	µs
		C_L = 1 µF	—	—	546	—	
		C_L = 1.5 µF	—	—	546	—	
I_{DDA} (V_{REFBUF})	V_{REFBUF} consumption from V_{DDA}	I_{LOAD} = 0 µA	—	—	75.4	88.4	µA
		I_{LOAD} = 500 µA	—	—	75.7	88.8	
		I_{LOAD} = 4 mA	—	—	75.8	89.1	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase	—		—	11	—	mA
$Regu_{(LINE)}$	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	—	236	—	ppm /V
			I_{load} = 4 mA	—	264	—	
$Regu_{(LOAD)}$	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal mode	—	66	—	ppm / mA
T_{COEFF}	Temperature drift	−40 °C < T_J < +125 °C		—	—	$T_{COEFF(VREFINT)}$ +30	ppm / °C
PSRR	Power supply rejection	DC	—	—	65	—	dB
		100 kHz	—	—	35	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

4.19. CMP characteristics

Table 4-48. CMP characteristics[1]

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>V_{DDA}</td><td>Operating voltage</td><td colspan="2">—</td><td>1.71</td><td>3.3</td><td>3.6</td><td>V</td></tr>
<tr><td>V_{IN}</td><td>Input voltage range</td><td colspan="2">—</td><td>0</td><td>—</td><td>V_{DDA}</td><td>V</td></tr>
<tr><td>V_{SC}</td><td>Scaler offset voltage</td><td colspan="2">—</td><td>—</td><td>3.5</td><td>11</td><td>mV</td></tr>
<tr><td rowspan="2">$I_{DDA(SCALER)}$</td><td rowspan="2">Scaler static consumption from V_{DDA}</td><td colspan="2">BRG_EN=0 (bridge disable)</td><td>—</td><td>200</td><td>226</td><td rowspan="2">μA</td></tr>
<tr><td colspan="2">BRG_EN=1 (bridge enable)</td><td>—</td><td>800</td><td>942</td></tr>
<tr><td>t_{START_SCALER}</td><td>Scaler startup time</td><td colspan="2">—</td><td>—</td><td>—</td><td>120</td><td>μs</td></tr>
<tr><td rowspan="6">t_D[2]</td><td rowspan="3">Propagation delay for 200 mV step with 100 mV overdrive</td><td colspan="2">Ultra-low power mode</td><td>—</td><td>612</td><td>1217</td><td>ns</td></tr>
<tr><td colspan="2">Medium power mode</td><td>—</td><td>102</td><td>165</td><td>ns</td></tr>
<tr><td colspan="2">High speed power mode</td><td>—</td><td>32.4</td><td>54</td><td>ns</td></tr>
<tr><td rowspan="3">Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs</td><td colspan="2">Ultra-low power mode</td><td>—</td><td>930</td><td>1650</td><td>ns</td></tr>
<tr><td colspan="2">Medium power mode</td><td>—</td><td>127</td><td>178</td><td>ns</td></tr>
<tr><td colspan="2">High speed power mode</td><td>—</td><td>35.4</td><td>58</td><td>ns</td></tr>
<tr><td rowspan="3">t_{START}</td><td rowspan="3">Comparator startup time to reach propagation delay specification</td><td colspan="2">High-speed mode</td><td>—</td><td>—</td><td>1.4</td><td rowspan="3">μs</td></tr>
<tr><td colspan="2">Medium mode</td><td>—</td><td>—</td><td>2.1</td></tr>
<tr><td colspan="2">Ultra-low-power mode</td><td>—</td><td>—</td><td>11.6</td></tr>
<tr><td rowspan="6">$I_{DDA(CMP)}$</td><td rowspan="6">Current consumption from V_{DDA}</td><td rowspan="2">Ultra-low power mode</td><td>Static</td><td>—</td><td>419</td><td>434</td><td rowspan="2">nA</td></tr>
<tr><td>With 50 kHz ±100 mV overdrive square signal</td><td>—</td><td>1890</td><td>—</td></tr>
<tr><td rowspan="2">Medium power mode</td><td>Static</td><td>—</td><td>4.25</td><td>4.30</td><td rowspan="4">μA</td></tr>
<tr><td>With 50 kHz ±100 mV overdrive square signal</td><td>—</td><td>3.95</td><td>—</td></tr>
<tr><td rowspan="2">High speed power mode</td><td>Static</td><td>—</td><td>45.4</td><td>46.2</td></tr>
<tr><td>With 50 kHz ±100 mV overdrive square signal</td><td>—</td><td>40.5</td><td>—</td></tr>
<tr><td>V_{offset}</td><td>Offset error</td><td colspan="2">—</td><td>—</td><td>4</td><td>18</td><td>mV</td></tr>
<tr><td rowspan="4">V_{hyst}</td><td rowspan="4">Hysteresis Voltage</td><td colspan="2">No Hysteresis</td><td>—</td><td>0</td><td>—</td><td rowspan="4">mV</td></tr>
<tr><td colspan="2">Low Hysteresis</td><td>7</td><td>10</td><td>17</td></tr>
<tr><td colspan="2">Medium Hysteresis</td><td>15</td><td>20</td><td>34</td></tr>
<tr><td colspan="2">High Hysteresis</td><td>23</td><td>30</td><td>52</td></tr>
</table>

(1) Value guaranteed by design, not 100% tested in production.
(2) Value guaranteed by characterization, not 100% tested in production.

4.20. Temperature and VBAT monitoring

Table 4-49. VBAT monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for VBAT	—	25	—	kΩ
Q	Ratio on VBAT measurement	—	4	—	—
Er	Error on Q	-10	—	+10	%
$t_{SAMPLE(VBAT)}$	ADC sampling time when reading VBAT input	10	—	—	μs
$V_{BAT(high)}$	High supply monitoring	—	3.56	—	V
$V_{BAT(low)}$	Low supply monitoring	—	1.36	—	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-50. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VCRSEL = 0	—	5	—	kΩ
		VCRSEL = 1	—	1.5	—	

Table 4-51. Temperature monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	—	120	—	°C
$TEMP_{low}$	Low temperature monitoring	—	-27	—	

(1) Value guaranteed by design, not 100% tested in production.

4.21. DAC characteristics

Table 4-52. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—		1.8	3.3	3.6	V
V_{REFP}	Positive Reference Voltage	—		1.8	—	V_{DDA}	V
V_{REFN}	Negative Reference Voltage	—		—	V_{SSA}	—	V
R_{LOAD}(1)	Resistive load	Resistive load with buffer ON	connected to V_{SSA}	5	—	—	kΩ
			connected to V_{DDA}	5	—	—	
R_{O}(1)	Impedance output	Impedance output with buffer OFF		—	—	15	kΩ
R_{BON}(1)	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON		—	—	1.5	kΩ
R_{BOFF}(1)	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF		—	—	1.5	

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Unit</th></tr>
<tr><td>C_{LOAD}(1)</td><td rowspan="2">Capacitive load</td><td colspan="2">DAC output buffer ON</td><td>—</td><td>—</td><td>50</td><td>pF</td></tr>
<tr><td>C_{SH}(1)</td><td colspan="2">Sample and Hold mode</td><td>—</td><td>0.1</td><td>1</td><td>μF</td></tr>
<tr><td rowspan="2">V_{DAC_OUT}</td><td rowspan="2">Voltage on DAC_OUT output</td><td colspan="2">DAC output buffer ON</td><td>0.2</td><td>—</td><td>V_{DDA}-0.2</td><td>V</td></tr>
<tr><td colspan="2">DAC output buffer OFF</td><td>0</td><td>—</td><td>V_{DDA}-1LSB</td><td>V</td></tr>
<tr><td rowspan="5">$t_{SETTLING}$(1)</td><td rowspan="5">Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5 LSB, ±1 LSB, ±2 LSB, ±4 LSB, ± 8 LSB)</td><td rowspan="4">Normal mode, DAC output buffer ON, CL ≤ 50 pF, RL ≥ 5 kΩ</td><td>±1 LSB</td><td>—</td><td>1.06</td><td>—</td><td rowspan="5">μs</td></tr>
<tr><td>±2 LSB</td><td>—</td><td>0.38</td><td>—</td></tr>
<tr><td>±4 LSB</td><td>—</td><td>0.33</td><td>—</td></tr>
<tr><td>±8 LSB</td><td>—</td><td>0.30</td><td>—</td></tr>
<tr><td colspan="2">Normal mode, DAC output buffer OFF, ±1LSB CL = 10 pF</td><td>—</td><td>1.95</td><td>2.5</td></tr>
<tr><td rowspan="2">t_{WAKEUP}(1)</td><td rowspan="2">Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of ±1 LSB is reached</td><td colspan="2">Normal mode, DAC output buffer ON, CL ≤ 50 pF, RL = 5 kΩ</td><td>—</td><td>5</td><td>10</td><td rowspan="2">μs</td></tr>
<tr><td colspan="2">Normal mode, DAC output buffer OFF, CL ≤ 10 pF</td><td>—</td><td>2</td><td>5</td></tr>
<tr><td>PSRR</td><td>Power supply rejection ratio(to V_{DDA})</td><td colspan="2">No R_{Load}, C_{LOAD} = 50 pF</td><td>50</td><td>70</td><td>—</td><td>dB</td></tr>
<tr><td rowspan="3">t_{SAMP}(1)</td><td rowspan="3">Sampling time in Sample and Hold mode C_L = 100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1LSB final value)</td><td colspan="2">MODE<2:0>_V12 = 100 / 101 (BUFFER ON)</td><td>—</td><td>0.8</td><td>1.1</td><td rowspan="2">ms</td></tr>
<tr><td colspan="2">MODE<2:0>_V12 = 110 (BUFFER OFF)</td><td>—</td><td>9.20</td><td>10.5</td></tr>
<tr><td colspan="2">MODE<2:0>_V12 = 111 (INTERNAL BUFFER OFF)</td><td>—</td><td>1.75</td><td>2.30</td><td>μs</td></tr>
<tr><td>C_{lint}</td><td>Internal sample and hold capacitor</td><td colspan="2">—</td><td>5.5</td><td>7</td><td>8.5</td><td>pF</td></tr>
<tr><td>t_{TRIM}</td><td>Middle code offset trim time</td><td colspan="2">Minimum time to verify the each code</td><td>100</td><td>—</td><td>—</td><td>μs</td></tr>
<tr><td rowspan="2">V_{offset}</td><td rowspan="2">Middle code offset for 1 trim code step</td><td colspan="2">V_{REFP} = 3.6 V</td><td>—</td><td>870</td><td>—</td><td rowspan="2">μV</td></tr>
<tr><td colspan="2">V_{REFP} = 1.8 V</td><td>—</td><td>435</td><td>—</td></tr>
<tr><td rowspan="2">I_{DDA}(1)(2)</td><td rowspan="2">DAC current consumption in quiescent mode</td><td rowspan="2">DAC output buffer ON</td><td>No load, middle code (0x800)</td><td>—</td><td>330</td><td>—</td><td rowspan="2">μA</td></tr>
<tr><td>No load, worst code (0xF1C)</td><td>—</td><td>330</td><td>—</td></tr>
</table>

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		DAC output buffer OFF	No load, middle/ worst code (0x800)	—	1	—	
		Sample and Hold mode, C_{SH} = 100 nF		—	330*T_{ON}/ (T_{ON}+T_{OFF})	—	
$I_{DDVREFP}$(1)	DAC current consumption in quiescent mode	DAC output buffer ON	No load, middle code (0x800)	—	100	—	μA
			No load, worst code (0xF1C)	—	300	—	
		DAC output buffer OFF	No load, middle code (0x800)	—	85	—	
		Sample and Hold mode, Buffer ON, C_{SH} = 100 nF (middle code)		—	100*T_{ON}/ (T_{ON}+T_{OFF})	—	
		Sample and Hold mode, Buffer OFF, C_{SH} = 100 nF (middle code)		—	85*T_{ON}/ (T_{ON}+T_{OFF})	—	

(1) Value guaranteed by design, not 100% tested in production.

(2) T_{ON} is the refresh phase duration, while T_{OFF} is the hold phase duration. Refer to the product reference manual for more details.

Table 4-53. DAC accuracy

Symbol	Parameter	Test conditions		Min	Typ	Max	Unit
DNL(2)	Differential non linearity	DAC output buffer ON		—	—	±2	LSB
		DAC output buffer OFF		—	—	±2	
INL(2)	Integral non linearity	DAC output buffer ON		—	—	±4	LSB
		DAC output buffer OFF		—	—	±4	
Offset(1)	Offset error at code 0x800	DAC output buffer ON	V_{REFP} = 3.6 V	—	—	±15	LSB
			V_{REFP} = 1.8 V	—	—	±30	
		DAC output buffer OFF		—	—	±8	
OffsetCal(2)	Offset error at code 0x800 after factory calibration	DAC output buffer ON	V_{REFP} = 3.6 V	—	—	±6	
			V_{REFP} = 1.8 V	—	—	±8	
Gain(2)	Gain error	DAC output buffer ON		—	—	±0.5	%
		DAC output buffer OFF		—	—	±0.5	

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

4.22. I2C characteristics

Table 4-54. I2C characteristics(1)(2)

Symbol	Parameter	Conditions	Standard mode		Fast mode		Fast mode plus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	0.2	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	0.5	—	μs
$t_{SU(SDA)}$	SDA setup time	—	250	—	100	—	50	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0(3)	3450	0	900	0	450	ns
$t_{R(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	—	120	ns
$t_{F(SDA/SCL)}$	SDA and SCL fall time	—	—	300	—	300	—	120	ns
$t_{H(STA)}$	Start condition hold time	—	4.0	—	0.6	—	0.26	—	μs
$t_{SU(STA)}$	Repeated Start condition setup time	—	4.7	—	0.6	—	0.26	—	μs
$t_{SU(STO)}$	Stop condition setup time	—	4.0	—	0.6	—	0.26	—	μs
t_{BUFF}	Stop to Start condition time (bus free)	—	4.7	—	1.3	—	0.5	—	μs

(1) Value guaranteed by design, not 100% tested in production.

(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-6. I2C bus timing diagram

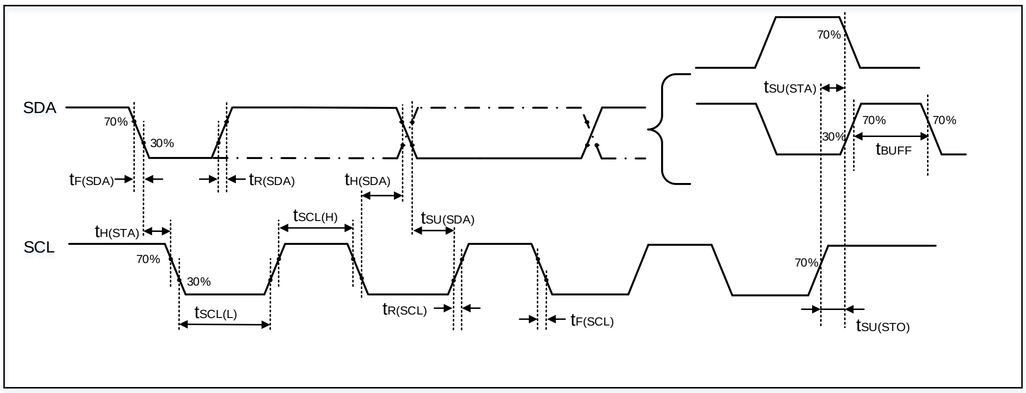


Table 4-55. I2C analog filter delay characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{AF}	Analog filter delay time	—	50	80	130	ns

(1) Value guaranteed by design, not 100% tested in production.

4.23. SPI characteristics

Table 4-56. Standard SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	125	MHz
$t_{SCK(H)}$	SCK clock high time	—	3	4	5	ns
$t_{SCK(L)}$	SCK clock low time	—	3	4	5	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	—	—	1	—	ns
$t_{H(MO)}$	Data output hold time	—	—	1	—	ns
$t_{SU(MI)}$	Data input setup time	—	3	—	—	ns
$t_{H(MI)}$	Data input hold time	—	3	—	—	ns
SPI slave mode						
$t_{SU(NSS)}$	NSS enable setup time	—	2	—	—	ns
$t_{H(NSS)}$	NSS enable hold time	—	1	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	13	—	ns
$t_{DIS(SO)}$	Data output disable time	—	—	1	—	ns
$t_{V(SO)}$	Data output valid time	—	—	8	—	ns
$t_{H(SO)}$	Data output hold time	—	—	7	—	ns
$t_{SU(SI)}$	Data input setup time	—	2	—	—	ns
$t_{H(SI)}$	Data input hold time	—	2	—	—	ns

(1) Value guaranteed by characterization, not 100% tested in production.

Figure 4-7. SPI timing diagram - master mode

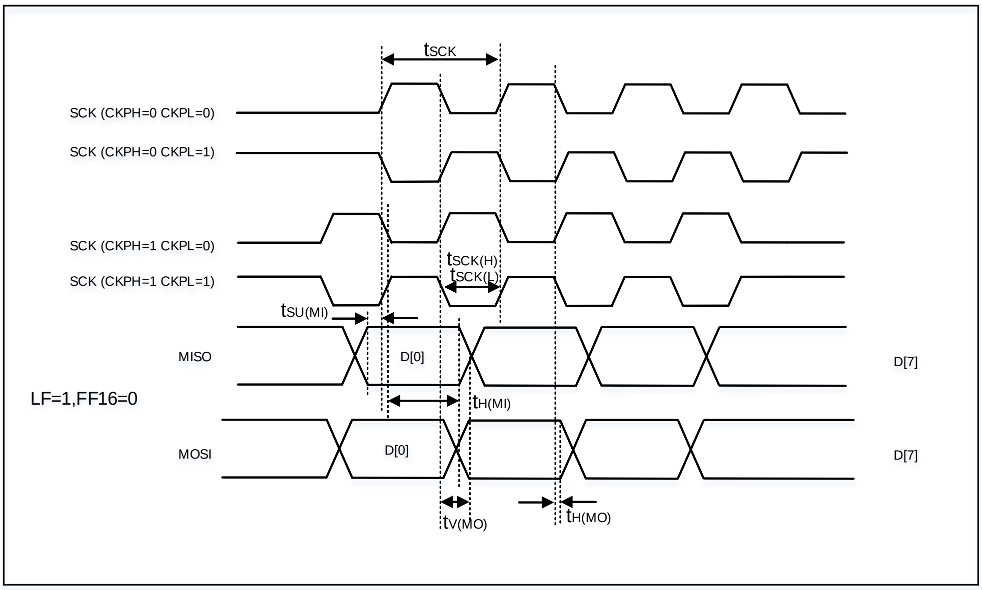
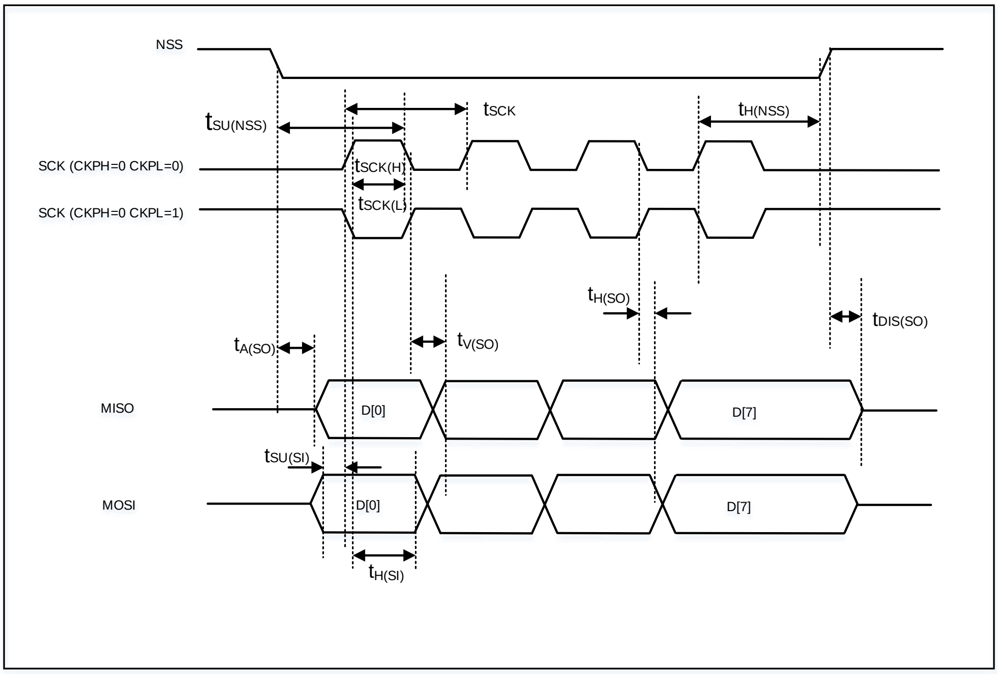


Figure 4-8. SPI timing diagram - slave mode



4.24. OSPI characteristics

Table 4-57. Standard OSPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SDR mode						
f_{SCK}	SCK clock frequency	—	—	—	100	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SCK(H)}$	SCK clock high time, even division	—	$t_{(CK)}$/2	—	$t_{(CK)}$/2+1	ns
	SCK clock high time, odd division	—	(n/2)*$t_{(CK)}$/(n+1)	—	(n/2)*$t_{(CK)}$/(n+1)+1	ns
$t_{SCK(L)}$	SCK clock low time, even division	—	$t_{(CK)}$/2–1	—	$t_{(CK)}$/2	ns
	SCK clock low time, odd division	—	(n/2+1)*$t_{(CK)}$/(n+1)–1	—	(n/2+1)*$t_{(CK)}$ /(n+1)	ns
$t_{V(MO)}$	Data output valid time	—	—	0.5	1	ns
$t_{H(MO)}$	Data output hold time	—	0	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	3.0	—	—	ns
$t_{H(MI)}$	Data input hold time	—	1.5	—	—	ns
DTR mode(no DQS)						
f_{SCK}	SCK clock frequency	—	—	—	57	MHz
$t_{SCK(H)}$	SCK clock high time, even division	—	$t_{(CK)}$/2	—	$t_{(CK)}$/2+1	ns
	SCK clock high time, odd division	—	(n/2)*$t_{(CK)}$/(n+1)	—	(n/2)*$t_{(CK)}$/(n+1)+1	ns
$t_{SCK(L)}$	SCK clock high time, even division	—	$t_{(CK)}$/2–1	—	$t_{(CK)}$/2	ns
	SCK clock high time, odd division	—	(n/2+1)*$t_{(CK)}$/(n+1)–1	—	(n/2+1)*$t_{(CK)}$ /(n+1)	ns
$t_{VR(SO)}$ $t_{VF(SO)}$	Data output valid time	DHQC = 0	—	6	7	ns
		DHQC = 1, Prescaler = 1,2 ...	—	t_{pclk}/4 + 1	t_{pclk}/4+1.25 (6)	
$t_{HR(SO)}$ $t_{HF(SO)}$	Data output hold time	DHQC = 0	4.5	—	—	ns
		DHQC = 1, Prescaler = 1,2 ...	t_{pclk}/4	—	—	
$t_{SUR(SI)}$ $t_{SUF(SI)}$	Data input setup time	—	3.0	—	—	ns
$t_{HR(SI)}$ $t_{HF(SI)}$	Data input hold time	—	1.50	—	—	ns

(1) Value guaranteed by characterization, not 100% tested in production.

Figure 4-9. OSPI timing diagram - SDR mode

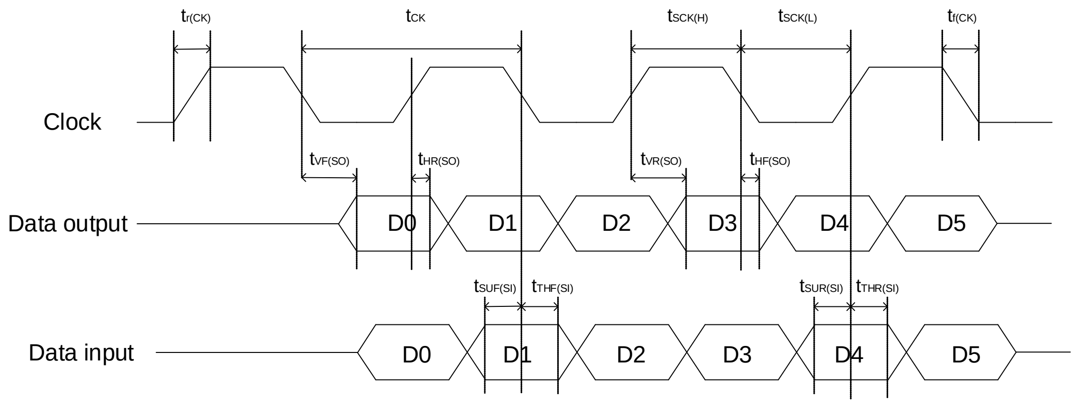
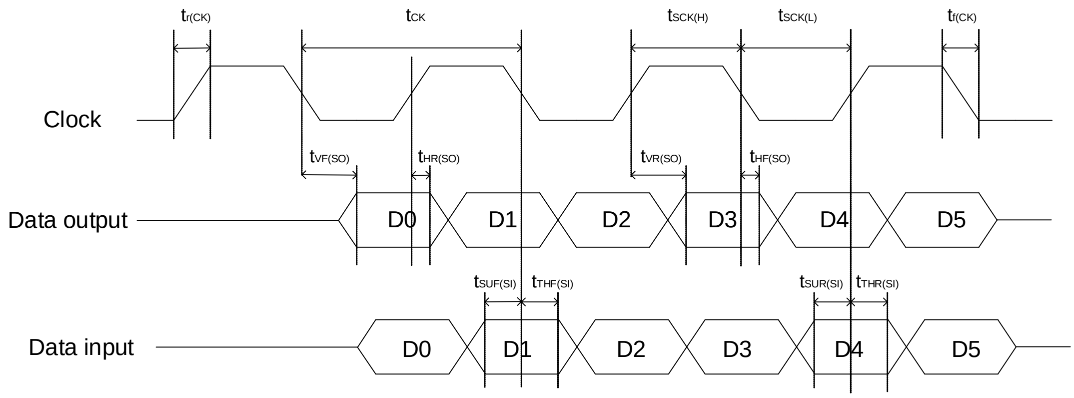


Figure 4-10. OSPI timing diagram - DTR mode



4.25. CPDM characteristics

Table 4-58. CPDM characteristics

Symbol	Parameter	Conditions	Min(2)	Typ(1)	Max(2)	Unit
t_{init}	Initial delay	—	2	TBD	9	ps
t_{Δ}	Unit Delay	—	31	TBD	65	ps

(1) Value guaranteed by characterization, not 100% tested in production.

(2) Value guaranteed by design, not 100% tested in production.

4.26. HPDF characteristics

Table 4-59. HPDF characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{HPDFCLK}$	HPDF clock	—	—	f_{APB2}	f_{SYSCLK}	MHz
f_{CKIN} (1 / T_{CKIN})	Input clock frequency	SPI mode(SITYP[1:0] = 01)	—	—	20 ($f_{HPDFCLK}$ / 4)	
f_{CKOUT}	Output clock	—	—	—	20	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	frequency					
$Duty_{CKOUT}$	Output clock frequency duty cycle	—	30	50	75	%
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode(SITYP[1:0] = 01), External clock mode(SPICKSS[1:0] = 0)	T_{CKIN} / 2-0.5	T_{CKIN} / 2	—	ns
t_{SU}	Data input setup time	SPI mode(SITYP[1:0] = 01), External clock mode(SPICKSS[1:0] = 0)	1	—	—	
t_h	Data input hold time	SPI mode(SITYP[1:0] = 01), External clock mode(SPICKSS[1:0] = 0)	1	—	—	
$T_{Manchester}$	Manchester data period(recovered clock period)	Manchester mode(SITYP[1:0] = 10 or 11), Internal clock mode(SPICKSS[1:0] ≠ 0)	(CKOUTDIV+1)*$T_{HPDFCLK}$	—	(2*CKOUTDIV)*$T_{HPDFCLK}$	

(1) Value guaranteed by design, not 100% tested in production.
(2) Output speed is set to OSPEEDRy[1:0] = 10; Capacitive load C = 30 pF; Measurement points are done at COMS levels: 0.5 * V_{DD}.

4.27. SAI characteristics

Table 4-60. SAI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCK}	SAI Main clock output	—	—	—	50	MHz
f_{CK}	SAI clock frequency	Master transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	—	—	45	
		Master transmitter, 1.71 V ≤ V_{DD} ≤ 3.6 V	—	—	32	
		Master receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	—	—	32	
		Slave transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	—	—	47.5	
		Slave transmitter, 1.71 V ≤ V_{DD} ≤ 3.6 V	—	—	41.5	
		Slave receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	—	—	50	

(1) Value guaranteed by design, not 100% tested in production.

4.28. I2S characteristics

Table 4-61. I2S characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	Clock frequency	Master mode (data: 32 bits, Audio frequency = 96 kHz)	—	6.25	—	MHz
		Slave mode	—	—	12.5	
t_H	Clock high time	—	—	80	—	ns
t_L	Clock low time		—	80	—	ns
$t_{V(WS)}$	WS valid time	Master mode	—	3	—	ns
$t_{H(WS)}$	WS hold time	Master mode	—	3	—	ns
$t_{SU(WS)}$	WS setup time	Slave mode	0	—	—	ns
$t_{H(WS)}$	WS hold time	Slave mode	3	—	—	ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode	—	50	—	%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	0	—	—	ns
$t_{su(SD\_SR)}$	Data input setup time	Slave mode	0	—	—	ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	1	—	—	ns
$t_{H(SD\_SR)}$		Slave receiver	3	—	—	ns
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	—	—	9	ns
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	6	—	—	ns
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	—	—	6	ns
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

(2) Value guaranteed by characterization, not 100% tested in production.

Figure 4-11. I2S timing diagram - master mode

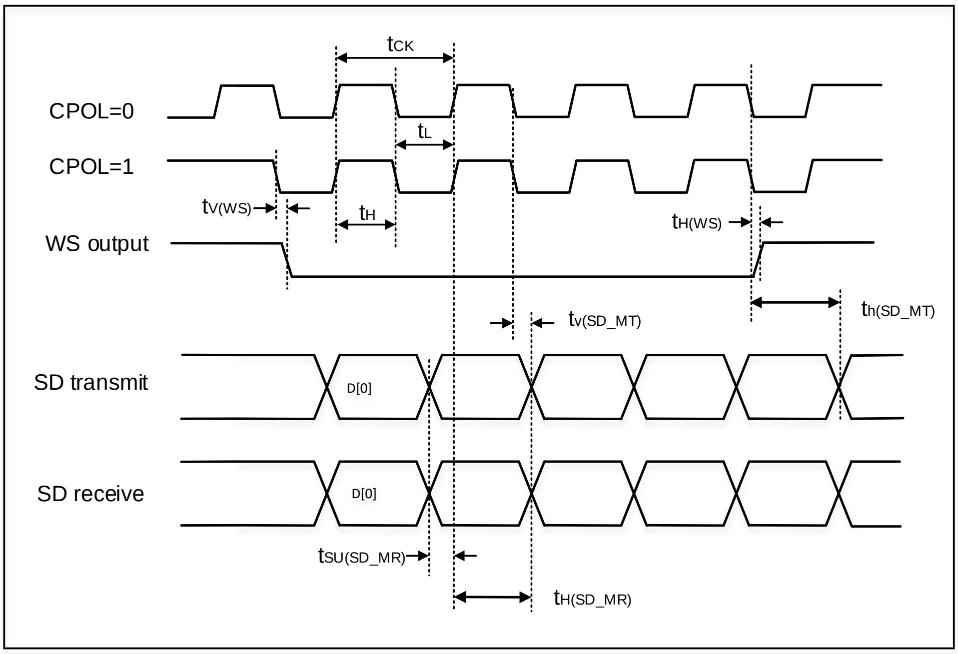
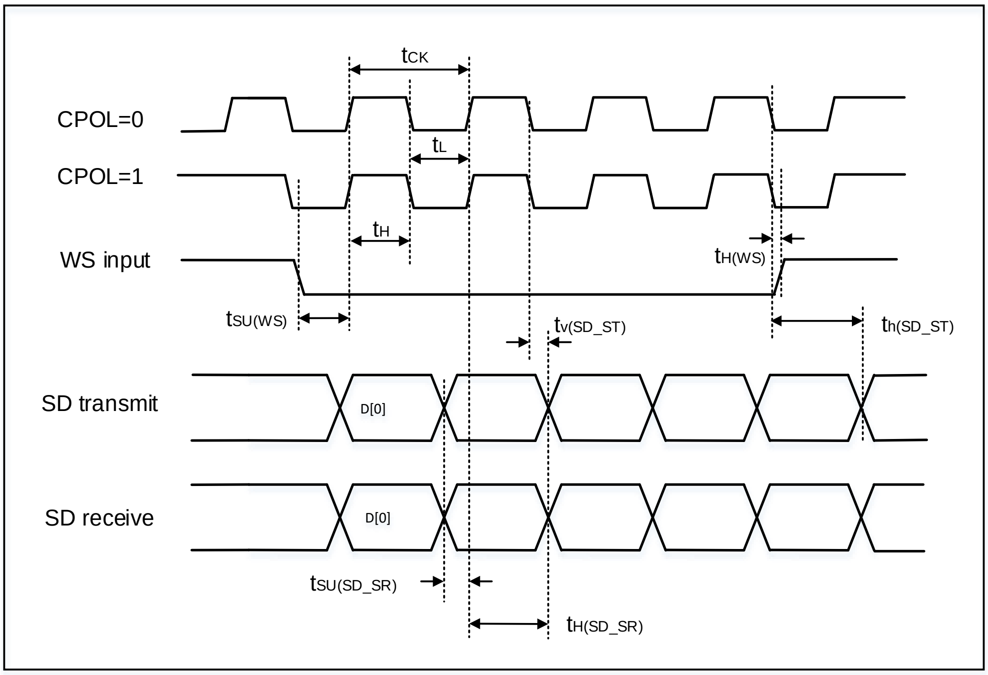


Figure 4-12. I2S timing diagram - slave mode



4.29. USART characteristics

Table 4-62. USART characteristics in Synchronous mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Fplckx = 300 MHz	—	—	37.5	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SCK(H)}$	SCK clock high time	Fplckx = 300 MHz	13.3	—	—	ns
$t_{SCK(L)}$	SCK clock low time	Fplckx = 300 MHz	13.3	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Table 4-63. USART characteristics in Smartcard mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	Fplckx = 300 MHz	—	—	150	MHz
$t_{SCK(H)}$	SCK clock high time	Fplckx = 300 MHz	3.33	—	—	ns
$t_{SCK(L)}$	SCK clock low time	Fplckx = 300 MHz	3.33	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.30. SDIO characteristics

Table 4-64. SDIO characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}(3)	Clock frequency in data transfer mode	—	0	—	120	MHz
$t_{W(CKL)}$ (3)	Clock low time	f_{pp} = 52 MHz	—	9.63	—	ns
$t_{W(CKH)}$ (3)	Clock high time	f_{pp} = 52 MHz	—	9.58	—	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}(4)	Input setup time HS	—	3	—	—	ns
t_{IH}(4)	Input hold time HS	—	1	—	—	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}(3)	Output valid time HS	—	—	5.5	6	ns
t_{OH}(3)	Output hold time HS	—	4	—	—	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}(4)	Input setup time SD	—	2	—	—	ns
t_{IHD}(4)	Input hold time SD	—	1	—	—	ns
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}(3)	Output valid default time SD	—	—	1	1	ns
t_{OHD}(3)	Output hold default time SD	—	0	—	—	ns

(1) CLK timing is measured at 50% of V_{DD}.
(2) Capacitive load C_L = 30 pF.
(3) Value guaranteed by characterization, not 100% tested in production.
(4) Value guaranteed by design, not 100% tested in production.

4.31. CAN characteristics

Refer to ***Table 4-27. I/O static characteristics*** for more details on the input/output alternate function characteristics (CANTX and CANRX).

4.32. USBHS characteristics

Table 4-65. USBHS DC electrical characteristics(1)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}		USB operating voltage	—	3	—	3.6	V
LS/FS FUNCTIONALITY							
Input levels	V_{DIFS}	Differential input sensitivity(FS / LS)	—	0.2	—	—	V
	V_{CMFS}	Differential common mode range(FS / LS)	Includes V_{DI} range	0.8	—	2.5	V
	V_{ILSE}	Single ended receiver low level input voltage(FS / LS)	—	—	—	0.8	V
	V_{IHSE}	Single ended receiver high level input voltage(FS / LS)	—	2.0	—	—	V
Output levels	V_{OLFS}	Static output level low(FS / LS)	R_L of 1.0 kΩ to 3.63 V	—	—	0.3	V
	V_{OHFS}	Static output level high(FS / LS)	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.6	V
R_{PD}		USBHS_DM/DP	V_{IN} = V_{DD}	17.6	21	24.7	kΩ
		PA9(USBHS_VBUS)		0.77	0.9	1.1	kΩ
R_{PU}		USBHS_DM/DP	V_{IN} = V_{SS}	1.3	1.5	1.83	kΩ
		PA9(USBHS_VBUS)		0.28	0.3	0.42	kΩ
Z_{HSDRV}		Driver Output Impedance	Steady state drive	40.5	45	49.5	Ω
HS FUNCTIONALITY							
Input levels	V_{DIHS}	Differential input sensitivity(HS)	—	0.1	—	—	V
	V_{CMHS}	Differential common mode range(HS)	—	-50	—	500	mV
	V_{HSSQ}	HS Squelch Detection Threshold	—	100	—	150	mV
	V_{HSDSC}	HS Disconnect Threshold	—	525	—	625	mV
Output levels	V_{OLHS}	High speed low level output voltage	45 Ω load	-10	—	10	mV
	V_{OHHS}	High speed high level output voltage	45 Ω load	360	400	440	mV

(1) Value guaranteed by design, not 100% tested in production.

Table 4-66. USBHS dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{FR}	Rise time(FS / LS)	C_L = 50 pF	4	5	20	ns
T_{HSR}	Differential Rise Time(HS)	—	500	600	—	ps
T_{FF}	Fall time(FS / LS)	C_L = 50 pF	4	5	20	ns
T_{HSF}	Differential Fall Time(HS)	—	500	600	—	ps
t_{RFM}	Rise/ fall time matching(FS / LS)	t_R / t_F	90	—	110	%
V_{CRS}	Output signal crossover voltage(FS / LS)	—	1.3	—	2.0	V

(1) Value guaranteed by design, not 100% tested in production.

Table 4-67. USBHS Charger Detection characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DAT_SRC}	Data Source Voltage	—	0.5	—	0.7	V
I_{DP_SRC}	Data Connect Current	—	7	—	13	uA
V_{DAT_REF}	Data Detect Voltage	—	0.25	—	0.4	V

(1) Value guaranteed by design, not 100% tested in production.

Table 4-68. USBHS clock timing parameters(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	USBHS operating voltage	3.0	—	3.63	V
f_{HCLK}	f_{HCLK} value to guarantee proper operation of USBHS interface	30	—	—	MHz
F_{START_8BIT}	Frequency (first transition) 8-bit ± 10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm	59.97	60	60.63	MHz
D_{START_8BIT}	Duty cycle (first transition) 8-bit ± 10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm	49.975	50	50.025	%

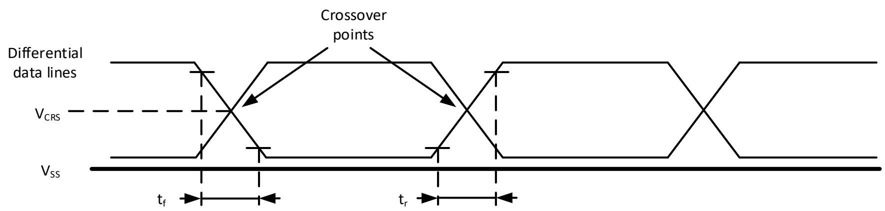
(1) Value guaranteed by design, not 100% tested in production.

Table 4-69. USB-ULPI Dynamic characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	—	—	2	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0.5	—	—	ns
t_{SD}	Data in setup time	—	—	2	ns
t_{HD}	Data in hold time	0	—	—	ns

(1) Value guaranteed by design, not 100% tested in production.

Figure 4-13. USBFS timings: definition of data signal rise and fall time



4.33. EXMC characteristics

Table 4-70. Asynchronous non-multiplexed SRAM / PSRAM / NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	5*Tfclk-1	5*Tfclk+1	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	0	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	5*Tfclk-1	5*Tfclk+1	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	4*Tfclk-1	—	ns

Symbol	Parameter	Min	Max	Unit
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	4*Tfclk-1	—	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	Tfclk-1	Tfclk+1	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-71. Asynchronous non-multiplexed SRAM / PSRAM / NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	3*Tfclk-1	3*Tfclk+1	ns
$t_{V(NWE\_NE)}$	EXMC_NEx low to EXMC_NWE low	Tfclk-1	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	Tfclk-1	Tfclk+1	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	Tfclk-1	Tfclk+1	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	Tfclk-1	Tfclk+1	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	2*Tfclk-1	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	Tfclk-1	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	Tfclk-1	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	0	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	Tfclk-1	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-72. Asynchronous multiplexed PSRAM / NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	7*Tfclk-1	7*Tfclk+1	ns
$t_{V(NOE\_NE)}$	EXMC_NEx low to EXMC_NOE low	3*Tfclk-1	—	ns
$t_{w(NOE)}$	EXMC_NOE low time	4*Tfclk-1	4*Tfclk+1	ns
$t_{h(NE\_NOE)}$	EXMC_NOE high to EXMC_NE high hold time	0	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{v(A\_NOE)}$	Address hold time after EXMC_NOE high	0	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{h(BL\_NOE)}$	EXMC_BL hold time after EXMC_NOE high	0	—	ns
$t_{su(DATA\_NE)}$	Data to EXMC_NEx high setup time	4*Tfclk-1	—	ns
$t_{su(DATA\_NOE)}$	Data to EXMC_NOEx high setup time	4*Tfclk-1	—	ns
$t_{h(DATA\_NOE)}$	Data hold time after EXMC_NOE high	0	—	ns
$t_{h(DATA\_NE)}$	Data hold time after EXMC_NEx high	0	—	ns
$t_{v(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	Tfclk-1	Tfclk+1	ns

Symbol	Parameter	Min	Max	Unit
$T_{h(AD\_NADV)}$	EXMC_AD(adress) valid hold time after EXMC_NADV high	Tfclk-1	Tfclk+1	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-73. Asynchronous multiplexed PSRAM / NOR write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	EXMC_NE low time	5*Tfclk-1	5*Tfclk+1	ns
$t_{V(NWE\_NE)}$	EXMC_NEx low to EXMC_NWE low	Tfclk-1	—	ns
$t_{w(NWE)}$	EXMC_NWE low time	3*Tfclk-1	3*Tfclk+1	ns
$t_{h(NE\_NWE)}$	EXMC_NWE high to EXMC_NE high hold time	Tfclk-1	—	ns
$t_{v(A\_NE)}$	EXMC_NEx low to EXMC_A valid	0	—	ns
$t_{V(NADV\_NE)}$	EXMC_NEx low to EXMC_NADV low	0	—	ns
$t_{w(NADV)}$	EXMC_NADV low time	Tfclk-1	Tfclk+1	ns
$t_{h(AD\_NADV)}$	EXMC_AD(address) valid hold time after EXMC_NADV high	Tfclk-1	—	ns
$t_{h(A\_NWE)}$	Address hold time after EXMC_NWE high	Tfclk-1	—	ns
$t_{h(BL\_NWE)}$	EXMC_BL hold time after EXMC_NWE high	Tfclk-1	—	ns
$t_{v(BL\_NE)}$	EXMC_NEx low to EXMC_BL valid	0	—	ns
$t_{v(DATA\_NADV)}$	EXMC_NADV high to DATA valid	Tfclk-1	—	ns
$t_{h(DATA\_NWE)}$	Data hold time after EXMC_NWE high	Tfclk-1	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-74. Synchronous multiplexed PSRAM / NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	Texmc_clk	—	ns
$t_{d(CLKL\text{-}NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH\text{-}NExH)}$	EXMC_CLK high to EXMC_NEx high	2*Tfclk-1	—	ns
$t_{d(CLKL\text{-}NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL\text{-}NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL\text{-}AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH\text{-}AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL\text{-}NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH\text{-}NOEH)}$	EXMC_CLK high to EXMC_NOE high	2*Tfclk-1	—	ns
$t_{d(CLKL\text{-}ADV)}$	EXMC_CLK low to EXMC_AD valid	0	—	ns
$t_{d(CLKL\text{-}ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-75. Synchronous multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	Texmc_clk	—	ns
$t_{d(CLKL\text{-}NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	2*Tfclk-1	—	ns
$t_{d(CLKL-ADIV)}$	EXMC_CLK low to EXMC_AD invalid	0	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-76. Synchronous non-multiplexed PSRAM / NOR read timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	Texmc_clk	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NOEL)}$	EXMC_CLK low to EXMC_NOE low	0	—	ns
$t_{d(CLKH-NOEH)}$	EXMC_CLK high to EXMC_NOE high	2*Tfclk-1	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-77. Synchronous non-multiplexed PSRAM write timings(1)(2)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	EXMC_CLK period	Texmc_clk	—	ns
$t_{d(CLKL-NExL)}$	EXMC_CLK low to EXMC_NEx low	0	—	ns
$t_{d(CLKH-NExH)}$	EXMC_CLK high to EXMC_NEx high	2*Tfclk-1	—	ns
$t_{d(CLKL-NADVL)}$	EXMC_CLK low to EXMC_NADV low	0	—	ns
$t_{d(CLKL-NADVH)}$	EXMC_CLK low to EXMC_NADV high	0	—	ns
$t_{d(CLKL-AV)}$	EXMC_CLK low to EXMC_Ax valid	0	—	ns
$t_{d(CLKH-AIV)}$	EXMC_CLK high to EXMC_Ax invalid	2*Tfclk-1	—	ns
$t_{d(CLKL-NWEL)}$	EXMC_CLK low to EXMC_NWE low	0	—	ns
$t_{d(CLKH-NWEH)}$	EXMC_CLK high to EXMC_NWE high	2*Tfclk-1	—	ns
$t_{d(CLKL-DATA)}$	EXMC_A/D valid data after EXMC_CLK low	0	—	ns
$t_{h(CLKL-NBLH)}$	EXMC_CLK low to EXMC_NBL high	0	—	ns

(1) C_L = 30 pF.
(2) Value guaranteed by design, not 100% tested in production.

Table 4-78. SDRAM read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	EXMC_SDCLK period	2 Tfclk − 0.5	2 Tfclk +0.5	ns
$t_{su(SDCLKH\_Data)}$	Data input setup time	3.5	—	
$t_{h(SDCLKH\_Data)}$	Data input hold time	0	—	
$t_{d(SDCLKL\_Add)}$	Address valid time	—	2.5	
$t_{d(SDCLKL- SDNE)}$	Chip select valid time	—	2.5	
$t_{h(SDCLKL\_SDNE)}$	Chip select hold time	0	—	
$t_{d(SDCLKL\_NRAS)}$	NRAS valid time	—	2	
$t_{h(SDCLKL\_NRAS)}$	NRAS hold time	0	—	
$t_{d(SDCLKL\_NCAS)}$	NCAS valid time	—	2	
$t_{h(SDCLKL\_NCAS)}$	NCAS hold time	0	—	

4.34. TIMER characteristics

Table 4-79. TIMER characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{res}	Timer resolution time	—	1	—	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	3.3	—	ns
f_{EXT}	Timer external clock frequency	—	0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 300 MHz	0	333	MHz
RES	Timer resolution	TIMER0 & TIMER2 & TIMER3 & TIMER7& TIMER14 & TIMER15 & TIMER16 & TIMER30 & TIMER31 & TIMER40 & TIMER41 & TIMER42 & TIMER43 & TIMER44	—	16	bit
		TIMER1 & TIMER4 & TIMER5 & TIMER6 & TIMER22 &	—	32	bit

Symbol	Parameter	Conditions	Min	Max	Unit
		TIMER23			
		TIMER50 & TIMER51	—	64	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	—	1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	0.0033	218.45	μs
	32-bit counter clock period when internal clock is selected	—	1	4294967296	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	0.0033	14316557.65	μs
	64-bit counter clock period when internal clock is selected	—	1	18446744073709551616	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	0.0033	61489146912365172.05	μs
t_{MAX_COUNT}	Maximum possible count（16-bit）	—	—	65536x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	—	14.3	s
	Maximum possible count (32-bit)	—	—	4294967296x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	—	938249.9	s
	Maximum possible count (64-bit)	—	—	18446744073709551616x65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 300 MHz	—	1119375758902.4	h

(1) Value guaranteed by design, not 100% tested in production.

4.35. DCI characteristics

Table 4-80. DCI characteristics(1)

Symbol	Parameter	Min	Max	Unit
Frequency ratio	DCI_PIXCLK /f_{HCLK}	—	0.4	
DCI_PIXCLK	Pixel clock input	—	160	MHz
D_{Pixel}	Pixel clock input duty cycle	30	70	%
$t_{su(DATA)}$	Data input setup time	2	—	ns
$t_{h(DATA)}$	Data output valid time	1	—	ns
$t_{su(HSYNC)}$	DCI_HS input setup time	2	—	ns
$t_{su(VSYNC)}$	DCI_VS input setup time	2	—	ns
$t_{h(HSYNC)}$	DCI_HS input hold time	1	—	ns
$t_{h(VSYNC)}$	DCI_VS input hold time	1	—	ns

(1) Value guaranteed by design, not 100% tested in production.

4.36. WDGT characteristics

Table 4-81. FWDGT min/max timeout period at 32 kHz (IRC32K) (1)

Prescaler divider	PR[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.03125	511.90625	ms
1/8	001	0.03125	1023.78125	
1/16	010	0.03125	2047.53125	
1/32	011	0.03125	4095.03125	
1/64	100	0.03125	8190.03125	
1/128	101	0.03125	16380.03125	
1/256	110 or 111	0.03125	32760.03125	

(1) Value guaranteed by design, not 100% tested in production.

Table 4-82. WWDGT min-max timeout value at 50 MHz (f_{PCLK1}) (1)

Prescaler divider	PSC[2:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	81.92	μs	5.24	ms
1/2	01	163.84		10.49	
1/4	10	327.68		20.97	
1/8	11	655.36		41.94	

(1) Value guaranteed by design, not 100% tested in production.

5. Package information

5.1. LQFP144 package outline dimensions

Figure 5-1. LQFP144 package outline

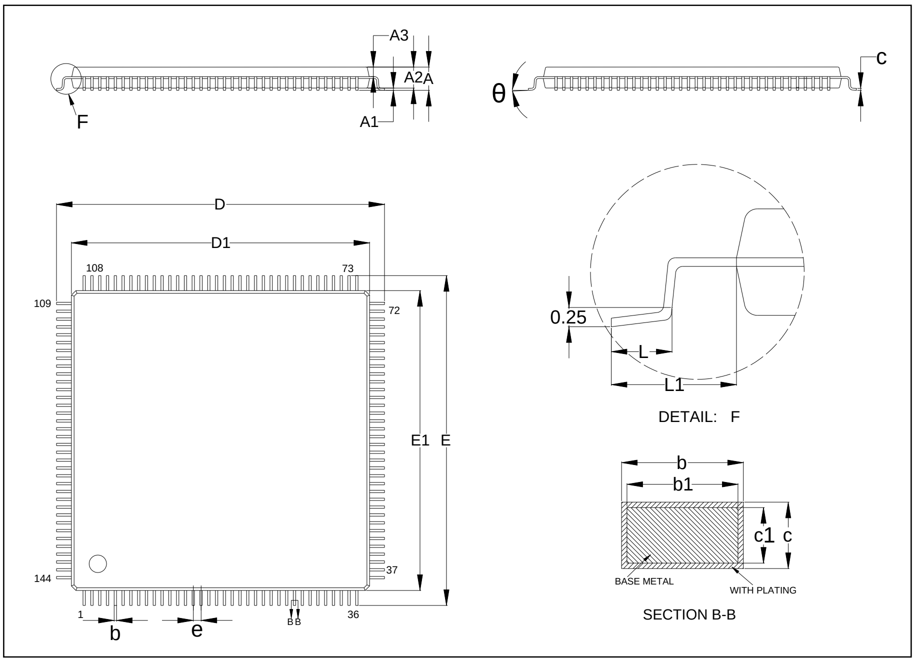
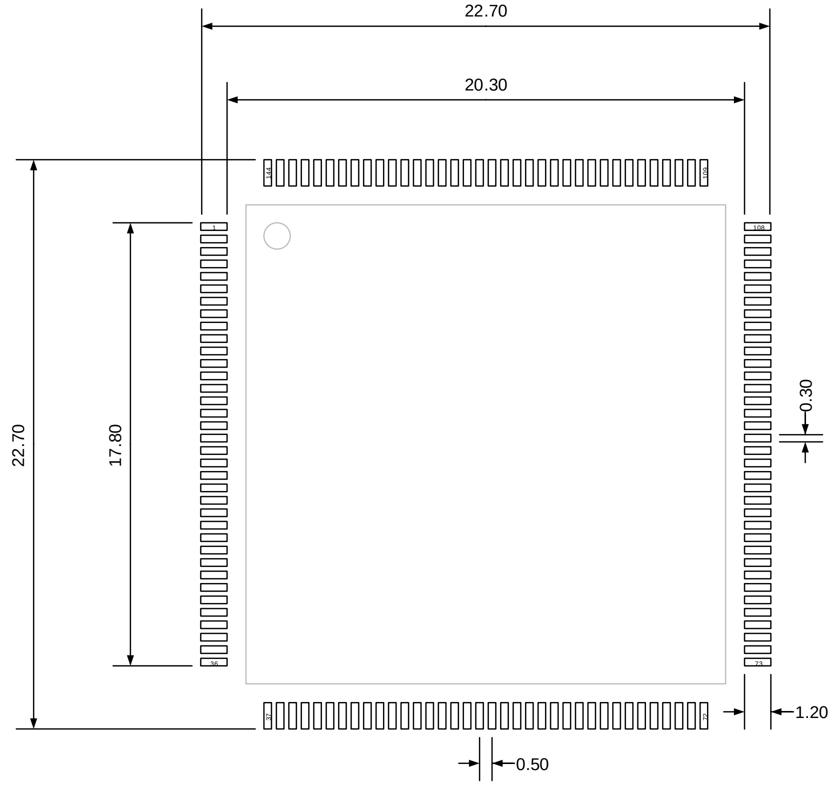


Table 5-1. LQFP144 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	—	0.50	—
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-2. LQFP144 recommended footprint



(Original dimensions are in millimeters)

5.2. BGA100 package outline dimensions

Figure 5-3. BGA100 package outline

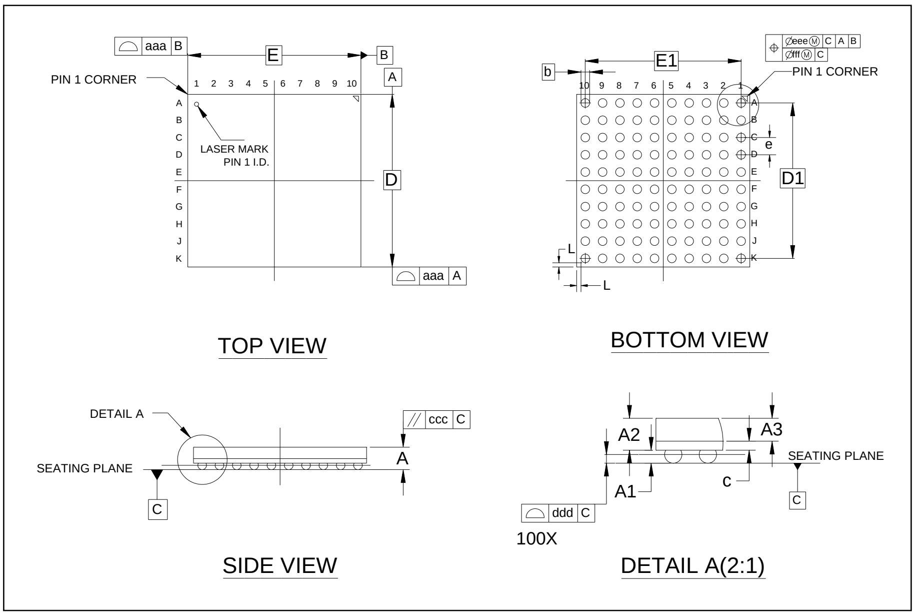
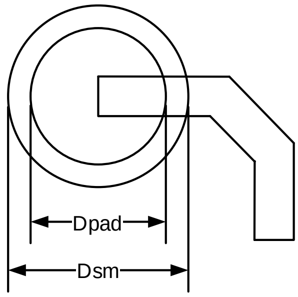


Table 5-2. BGA100 package dimensions

Symbol	Min	Typ	Max
A	0.98	1.04	1.10
A1	0.25	0.30	0.35
A2	0.69	0.74	0.79
A3	—	0.53	—
b	0.35	0.40	0.45
c	0.18	0.21	0.24
D	7.90	8.00	8.10
D1	—	7.20	—
E	7.90	8.00	8.10
E1	—	7.20	—
e	—	0.80	—
L	—	0.20	—
aaa	—	0.15	—
ccc	—	0.11	—
ddd	—	0.10	—
eee	—	0.15	—
fff	—	0.08	—

(Original dimensions are in millimeters)

Figure 5-4. BGA100 recommended footprint



Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.37 mm
Dsm	0.47 mm

(Original dimensions are in millimeters)

5.3. LQFP100 package outline dimensions

Figure 5-5. LQFP100 package outline

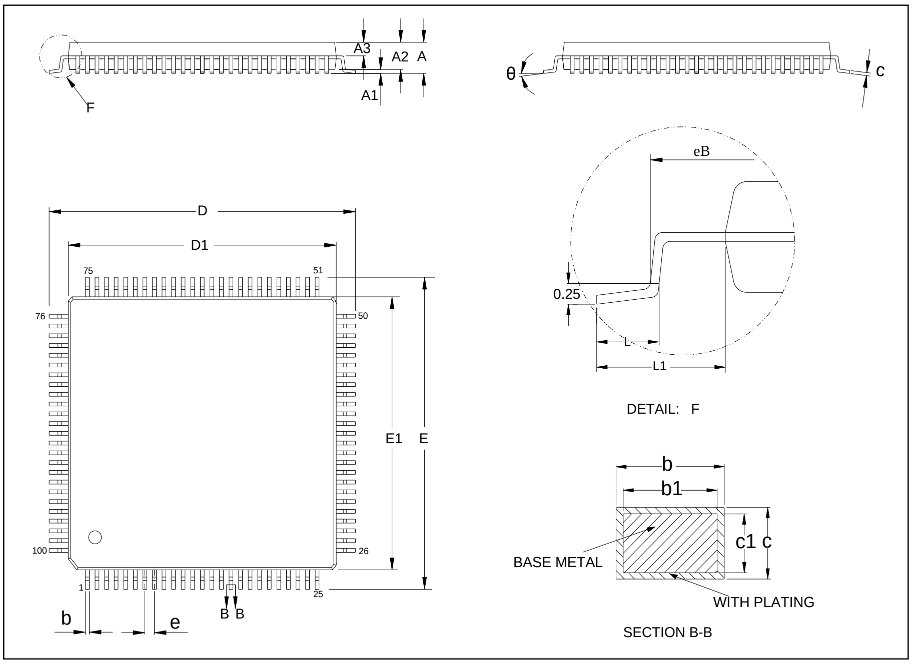
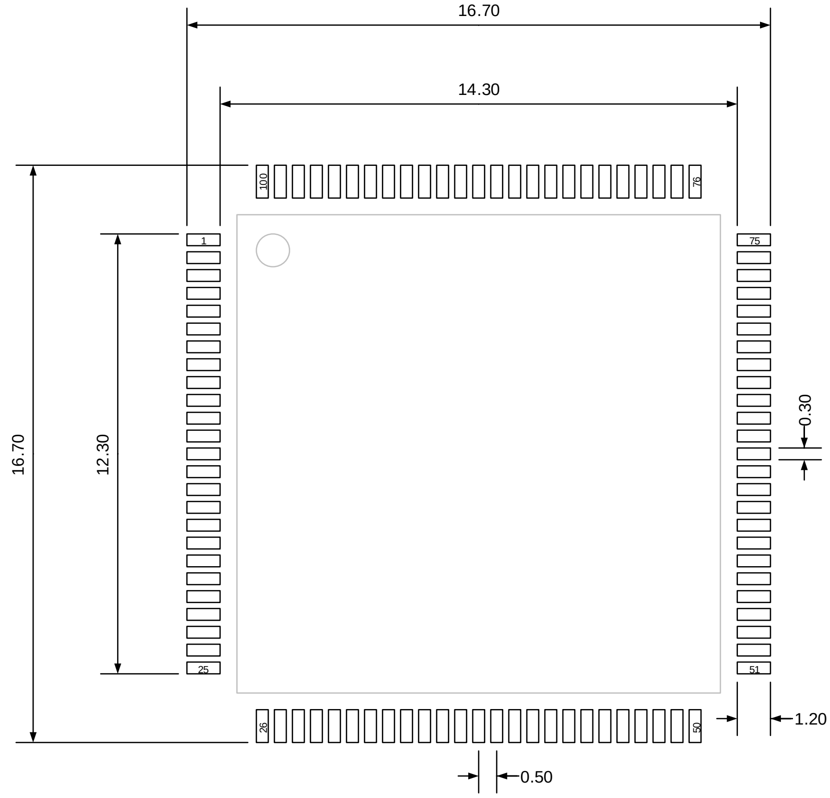


Table 5-3. LQFP100 package dimensions

Symbol	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	—	0.50	—
eB	15.05	—	15.35
L	0.45	—	0.75
L1	—	1.00	—
θ	0°	—	7°

(Original dimensions are in millimeters)

Figure 5-6. LQFP100 recommended footprint



(Original dimensions are in millimeters)

5.4. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA}: Thermal resistance, junction-to-ambient.

θ_{JB}: Thermal resistance, junction-to-board.

θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5\text{-}1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5\text{-}2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5\text{-}3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-4. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
θ_{JA}	Natural convection, 2S2P PCB	LQFP144	47.23	°C/W
		LQFP100	47.842	
		BGA100	49.20	
θ_{JB}	Cold plate, 2S2P PCB	LQFP144	34.38	°C/W
		LQFP100	33.877	
		BGA100	30.69	

Symbol	Condition	Package	Value	Unit
θ_{JC}	Cold plate, 2S2P PCB	LQFP144	10.09	°C/W
		LQFP100	7.428	
		BGA100	15.40	
Ψ_{JB}	Natural convection, 2S2P PCB	LQFP144	35.68	°C/W
		LQFP100	34.062	
		BGA100	30.61	
Ψ_{JT}	Natural convection, 2S2P PCB	LQFP144	0.58	°C/W
		LQFP100	0.33	
		BGA100	1.41	

(1): Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32H757xx devices

Ordering code	Flash (KB)	Package	Package type	Temperature operating range
GD32H757VGT6	1024	LQFP100	Green	Industrial -40°C to +85°C
GD32H757VIT6	2048	LQFP100	Green	Industrial -40°C to +85°C
GD32H757VMT6	3840	LQFP100	Green	Industrial -40°C to +85°C
GD32H757VGJ6	1024	BGA100	Green	Industrial -40°C to +85°C
GD32H757VIJ6	2048	BGA100	Green	Industrial -40°C to +85°C
GD32H757VMJ6	3840	BGA100	Green	Industrial -40°C to +85°C
GD32H757ZGT6	1024	LQFP144	Green	Industrial -40°C to +85°C
GD32H757ZIT6	2048	LQFP144	Green	Industrial -40°C to +85°C
GD32H757ZMT6	3840	LQFP144	Green	Industrial -40°C to +85°C

7. Revision history

Table 7-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	May.9, 2023
1.1	1. Update the ***Table 2-1. GD32H757xx devices features and peripheral list***. 2. Add the (3)/(4) comment for special pins in ***Table 2-3. GD32H757Zx LQFP144 pin definitions***, ***Table 2-4. GD32H757Vx LQFP100 pin definitions*** and ***Table 2-5. GD32H757Vx BGA100 pin definitions***. 3. Delete the description of SMPS in ***Table 4-42. Low power digital temperature sensor characteristics***. 4. Update the ***Table 4-15. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics (4)***. 5. Add the 5VT pin tolerance voltage information in ***Table 4-2. Absolute maximum ratings(1)(4)***. 6. Update the ***Table 4-42. Voltage reference buffer characteristics(1)***. 7. Add the parameters of EMC.	Jul.19, 2023
1.2	1. Update ***Table 4-46. Temperature monitoring characteristics(1)***. 2. Update ***Table 4-37. High-precision temperature sensor characteristics***. 3. Add ***Figure 4-2. Recommended PDR_ON pin circuit(1)***. 4. Update ***Table 4-8. Power consumption characteristics (1)(2)(3)(4)***. 6. Update ***Table 4-31. 14-bit ADC characteristics***.	Dec.27, 2023
1.3	1. Add ***Table 4-36. ADC dynamic accuracy at fADC = 60 MHz VREFP = 1.8 V***. 2. Add ***Table 4-37. ADC dynamic accuracy at fADC = 80 MHz VREFP = 2.4 V***. 3. Add ***Table 4-38. ADC dynamic accuracy at fADC = 80 MHz VREFP = 3.3 V***. 4. Add ***Table 4-39. ADC static accuracy at fADC = 60 MHz VREFP = 1.8 V***. 5. Add ***Table 4-40. ADC static accuracy at fADC = 80 MHz VREFP = 2.4 V***. 6. Add ***Table 4-41. ADC static accuracy at fADC = 80 MHz VREFP = 3.3 V***.	Mar.8, 2024

Important Notice