GigaDevice Semiconductor Inc.

Precautions for the use of USBHS of GD32H7xx series

Application Notes
AN117

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1. Foreword

This document is intended for GD32H7xx MCU and introduces precautions during USBHS development and use, including clock configuration, GPIO configuration, PHY configuration, power supply configuration, and other software configurations. For the hardware part of USBHS, please refer to ***Manual of Hardware Development of AN109 GD32H7xx Seriess.***

This application note aims to introduce operation keys of USBHS of GD32H7xx series, so that users can quickly know how to properly use USBHS.

Table 1-1. Applicable product

Type	Part Numbers
MCU	GD32H7xx Series

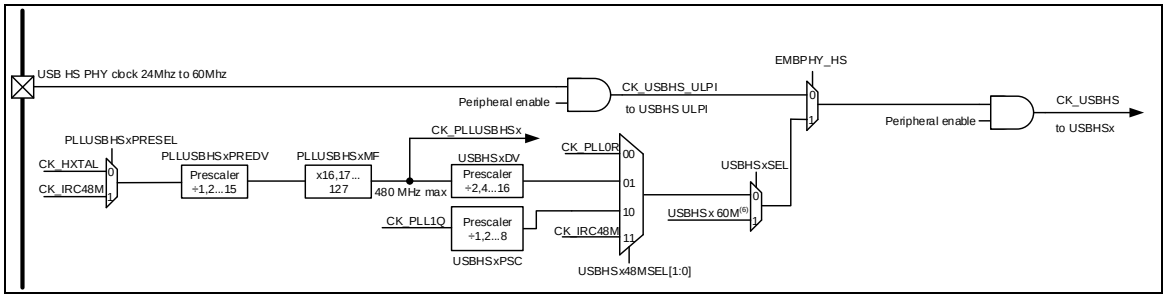
2. Precautions for the use of UBSHS

2.1. UBSHS clock configuration

2.1.1. Peripheral module clock

USBHS peripheral clock tree is as shown in ***Figure 2-1. USBHS clock*** tree.

Figure 2-1. USBHS clock tree



Internal PHY or external ULPI PHY can be selected through EMBPHY_HS selector. External ULPI PHY clock is provided by CLK signal wire of PHY, while internal PHY clock is generated inside MCU.

USBHSxSEL selector is used to select the clock source USBHSx60M or USBHSx48MSEL. USBHSx60M is obtained by dividing the 480M PHY clock. When selecting with software, it is required to set USBHSxSWEN bit of RCU_USBCLKCTL register. If USBHSxSWEN bit of RCU_USBCLKCTL register is 0, the clock source will be selected by the hardware by default. Hardware will select USBHSx60M as the clock source when chirp handshake results in high speed.

USBHSx48MSEL selector can select four clock sources as below (to be compatible with the full speed mode, it is recommended to configure the output clock of the selector as 48M):

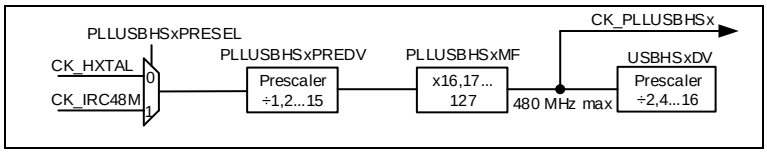
- CK_PLL0R: It is obtained through PLL0 frequency division.
- It is obtained through CK_PLLUSBHSx frequency division.
- CK_PLL1Q: It is obtained through PLL1 frequency division
- CK_IRC48M: provided by internal 48M clock (need to calibrate precision to ±500ppm)

2.1.2. Internal PHY clock

Configuration of internal PHY clock is as shown in ***Figure 2-2. Internal PHY clock*** tree. Clock source is CK_HXTAL or CK_IRC48M. As precision of IRC48M is not high, when the frequency is multiplied to 480M, larger error may lead to failure in pressure test, so it is recommended to use CK_HXTAL at high-speed status. By the clock divided from PLLUSBHSxPREDV and the clock multiplied from PLLUSBHSxMF, the CK_PLLUSBHSx clock frequency is 480M (HXTAL_VALUE / PLLUSBHSxPREDV * PLLUSBHSxMF = 480M).

Then, the 480M clock can be used by USBHS module through USBHSxDV frequency division.

Figure 2-2. Internal PHY clock tree

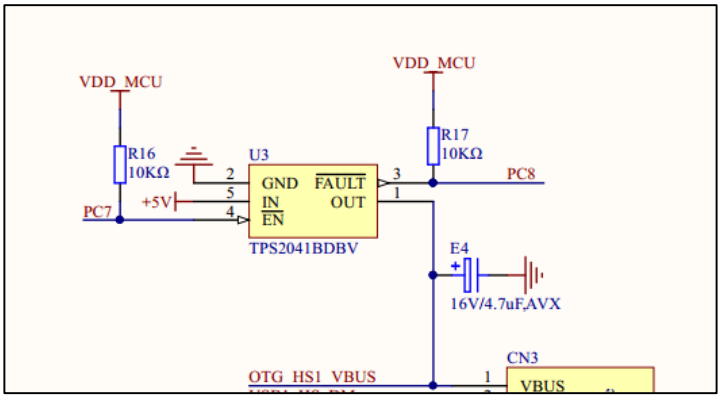


2.2. GPIO configuration of USBHS

When enabling ADP function, it is required to configure VBUS pins (PA9 (USBHS0), PB12 (USBHS1)) in analog mode. When enabling OTG function, it is required to configure ID pins (PA10 (USBHS0), PB13 (USBHS1)) in AF mode. Note that configuration is not required for dedicated DP/DM pin of USBHS. When using external ULPI PHY, it is required to configure related GPIO of ULPI communication in AF mode, and the detailed AF selection is determined by AFIO.

USBHS VBUS power supply is controlled by a switch IC as shown in ***Figure 2-3. USBHS VBUS Control Circuit***. 5V voltage on VBUS is controlled through the control signal PC7 (different development boards have different control pins). When working in USB host status, it is required to enable VBUS to provide 5V voltage externally.

Figure 2-3. USBHS VBUS Control Circuit



2.3. Internal and External PHY Configuration

GD32H7xx series include two internal USB PHYs, internal FS PHY and internal HS PHY, and provide support for external ULPI PHY. Detailed speed configuration is as shown in ***Table 2-1. USBHS-supported speed*** list.

Table 2-1. USBHS-supported speed list

Register configuration		Host supported speed	Device supported speed
EMBPHY_FS=1		Full-Speed	Full-Speed

Register configuration		Host supported speed	Device supported speed
EMBPHY_HS=0 (Internal FS PHY)		Low-Speed	
EMBPHY_FS=0 EMBPHY_HS=1 (Internal HS PHY)	DS = 01 (device mode) SPDFSLS = 1 (host mode)	Full-Speed Low-Speed	Full-Speed
	DS = 00 (device mode) SPDFSLS = 0 (host mode)	High-Speed Full-Speed Low-Speed	High-Speed Full-Speed
EMBPHY_FS=0 EMBPHY_HS=0 (External ULPI PHY)	DS = 01 (device mode) SPDFSLS = 1 (host mode)	Full-Speed Low-Speed	Full-Speed
	DS = 00 (device mode) SPDFSLS = 0 (host mode)	High-Speed Full-Speed Low-Speed	High-Speed Full-Speed

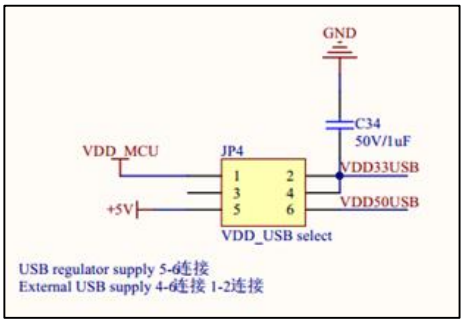
2.4. UBSHS power supply configuration

Operation of internal PHY of USBHS requires 3.3V working voltage, which can be provided in the following two ways in GD32H7xx series (for the schematic diagram, please refer to ***Figure 2-4. Control circuit of USBHS 3.3V working voltage***):

- **Externally supplying 3.3V**: In the case of hardware connection, short circuit VDD33USB and VDD50USB and input 3.3V voltage to VDD33USB pin (short circuit 4/6 and 1/2 of JP4); in the case of software configuration, set VUSB33DEN bit of PMU_CTL2 register and poll until USB33RF bit of PMU_CTL2 register is set.
- **Dedicated LDO conversion in USB**: In the case of hardware connection, input 5V voltage to VDD50USB (short circuit 5/6 of JP4); in the case of software configuration, set USBSEN bit and VUSB33DEN bit of PMU_CTL2 register and poll until USB33RF bit of PMU_CTL2 register is set.

Note: In the case of software configuration, it is required to place USBHS power supply configuration before PHY configuration.

Figure 2-4. Control circuit of USBHS 3.3V working voltage



2.5. Other precautions

- When using internal PHY, DP/DM pins of the data lines are not required to be connected with the matching resistor in series.
- When using external ULPI PHY, PHY is allowed to provide 60M clock signal to MCU, but MCU is not allowed to output 60M clock signal to PHY.
- When enabling DMA function of USBHS, avoid using D-Cache function.

3. Revision history

Table 3-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Apr. 11, 2023

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