GigaDevice Semiconductor Inc.

GD32F1x0 Hardware Development Guide

Application Note
AN108

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1. Introduction

This article is specially provided for developers of 32-bit general-purpose MCU GD32F1x0 series based on Arm® Cortex®-M3 architecture. It provides an overall introduction to the hardware development of GD32F1x0 series products, such as power supply, reset, clock, boot mode settings and download debugging. The purpose of this development guide is to allow developers to quickly get started and use GD32F1x0 series products, and quickly develop and use product hardware, save the time of studying manuals, and speed up product development progress.

This application note is divided into seven parts to describe:

1. Power supply, mainly introduces the design of GD32F1x0 series power management, power supply and reset functions.
2. Clock, mainly introduces the functional design of GD32F1x0 series high and low speed clocks.
3. Boot configuration, mainly introduces the BOOT configuration and design of GD32F1x0 series.
4. Typical peripheral modules, mainly introduces the hardware design of the main functional modules of the GD32F1x0 series.
5. Download and debug circuit, mainly introduces the recommended typical download and debug circuit of GD32F1x0 series.
6. Reference circuit and PCB Layout design, mainly introduces GD32F1x0 series hardware circuit design and PCB Layout design notes.
7. Package description, mainly introduces the package forms and names included in the GD32F1x0 series.

This document also satisfies the minimum system hardware resources used in application development based on GD32F1x0 series products.

Table 1-1. Applicable Products

Type	Part Numbers
MCU	GD32F130xx series
	GD32F150xx series

2.   Hardware design

2.1.   Power supply

The V_{DD} / V_{DDA} operating voltage range of GD32F130/GD32F150 series products is 2.6V ~ 3.6V. For GD32F130/GD32F150 series, there are three power domains, including V_{DD} / V_{DDA} domain, 1.2V domain, and Backup domain, as is shown in *__Figure 2-1.__* *__GD32F130/GD32F150 Power supply overview.__* The V_{DD}/V_{DDA} domain is powered directly by the power supply, and an LDO is embedded in the V_{DD}/V_{DDA} domain to power the 1.2V domain. The backup domain power supply V_{BAK} can be powered by V_{DD} or V_{BAT} through the power switch Power Switch. When the V_{DD} power supply is turned off, the power switch can switch the power supply of the backup domain to the V_{BAT} pin. At this time, the backup domain is powered by the V_{BAT} pin (battery).

Figure 2-1. GD32F130/GD32F150 Power supply overview

LVD: Low Voltage Detector   LDO: Voltage Regulator   BPOR: V_{BAK} Power On Reset
POR: Power On Reset   PDR: Power Down Reset
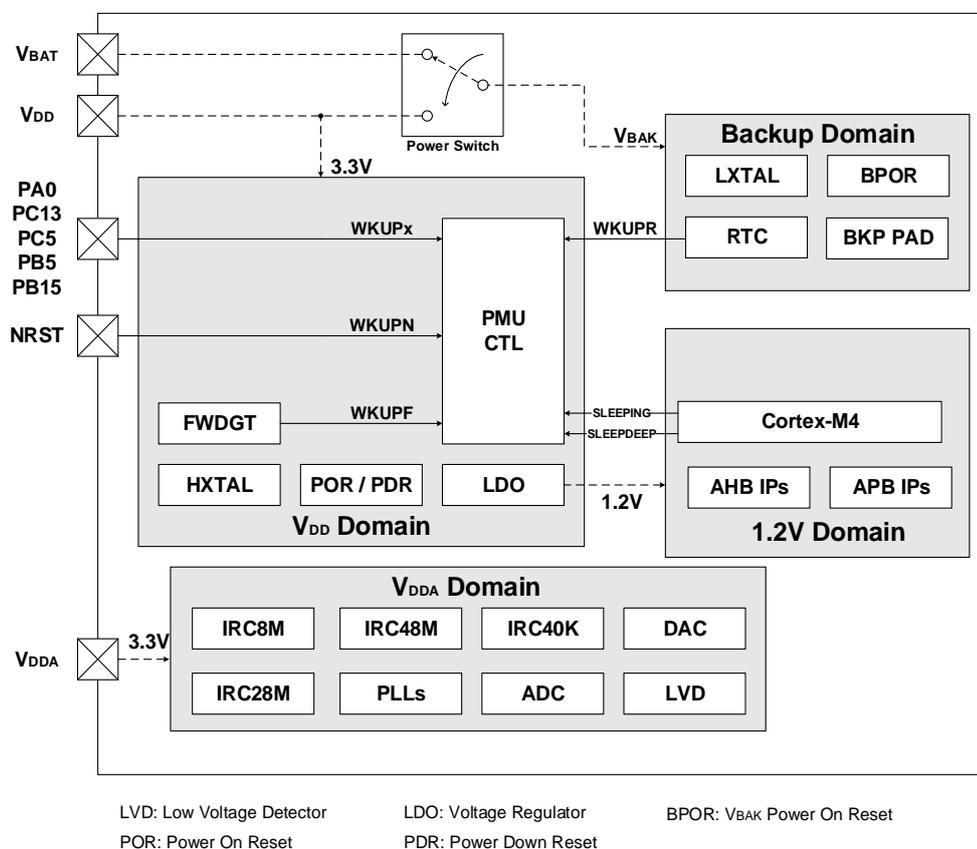
2.1.1.   Backup domain

The backup domain of GD32F130/GD32F150 series supply voltage range is 1.8V ~ 3.6V. In order to ensure the content of the Backup domain registers and the RTC supply, when VDD supply is shut down, VBAT pin can be connected to an optional standby voltage supplied by a battery or by another source. The power switch is controlled by the Power Down Reset

circuit in the VDD / VDDA domain. If no external battery is used in the application, it is recommended to connect VBAT pin externally to VDD pin with a 100nF external ceramic decoupling capacitor.

Note: If the VBAT pin is left floating, the Power Switch will switch VBAK to VDD after the MCU is powered on, and the internal VDD will directly supply power to the Backup domain.

2.1.2. V_{DD}/V_{DDA} Power domain

The V_{DD} / V_{DDA} power domain supplies power to all areas except the backup domain. If VDDA is not equal to VDD, the voltage difference between the two is required to be less than 300mV (the internal VDDA and VDD are connected by back-to-back diodes). To avoid noise, VDDA can be connected to VDD through an external filter circuit, and the corresponding VSSA can be connected to VSS through a specific circuit (single-point grounding, through 0Ω resistors or magnetic beads, etc.).

2.1.3.   Power supply design

The system needs a stable power supply. There are some important things to pay attention to when developing:

- The V_{DD} pin must be connected with an external capacitor (N*100nF ceramic capacitor + not less than 4.7uF tantalum capacitor, at least one V_{DD} needs to be connected to GND with a capacitor of not less than 4.7uF, and other V_{DD} pins are connected to 100nF).
- The V_{DDA} pin must be connected with an external capacitor (recommend 10nF+1uF ceramic capacitor).
- The V_{BAT} pin must be connected to an external battery (external battery voltage range of GD32F130/GD32F150 is 1.8V~3.6V). If there is no external battery, it is recommended to connect the VBAT pin to the ground through a 100nF capacitor and then connect it to the VDD pin.

Figure 2-2. GD32F1x0 series recommended power supply design

GD32F1x0
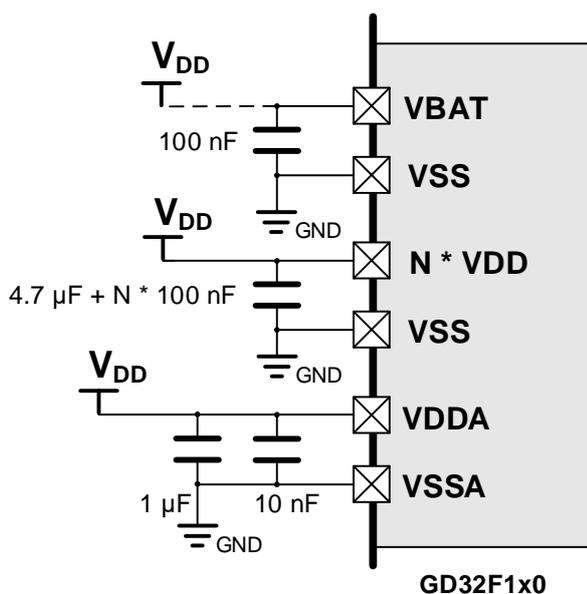
Note：

1、 All decoupling capacitors must be placed close to the corresponding VDD, VDDA, VBAT pins of the chip.
2、 VBAT can be directly connected to VDD, or can be connected to an external battery according to the actual application.

2.1.4.   Reset and power management

GD32F1x0 series reset control includes three resets: power reset, system reset and backup domain reset. A power reset is a cold reset, which resets all systems except the backup domain when the power is turned on. During the power and system reset process, NRST will maintain a low level until the reset is over. When the MCU cannot be executed, you can monitor the waveform of the NRST pin with an oscilloscope to determine whether the chip has been reset. The chip integrates a POR/PDR (power-on/power-down reset) circuit to detect V_{DD} / V_{DDA} and generate a power reset signal to reset the entire chip except the backup domain when the voltage is lower than a certain threshold. V_{POR}, indicates the threshold of power on reset, while V_{PDR} means the threshold of power down reset. The GD32F130/GD32F150 series can configure the V_{PDR} to 2.35V (1.8V), V_{POR} to 2.4V, and hysteresis voltage Vhyst value of about 50mV (600mV) by writing 0x1A2B3C4D to the RCU_VKEY register, and then configuring the RCU_PDVSEL register corresponding to bit position 0 (set 1).

Figure 2-3. Waveform of the POR / PDR
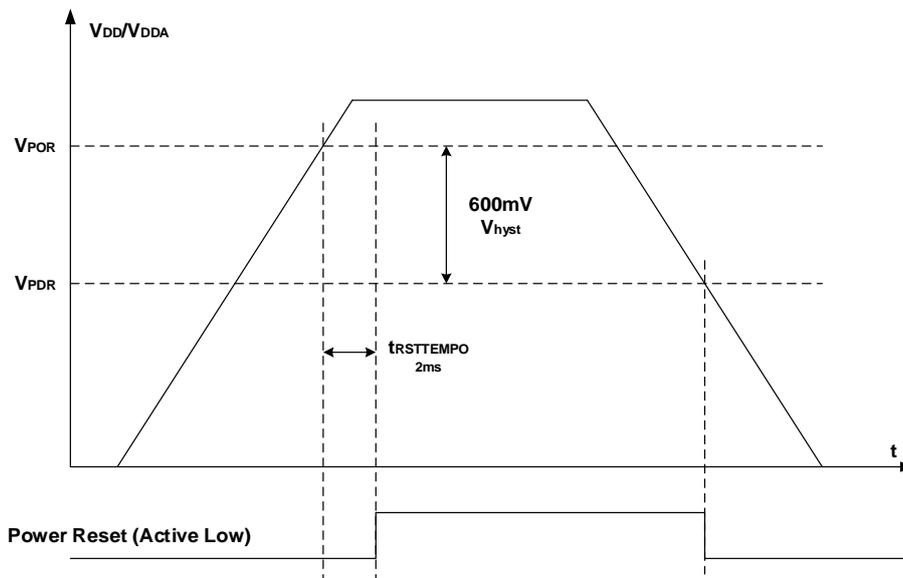
The LVD is used to detect whether the V_{DD} / V_{DDA} supply voltage (The GD32F130/GD32F150 series ranges from 2.2 V ~ 2.9 V) is lower than a programmed threshold selected by the LVDT[2:0] bits in the Power control register (PMU_CTL). The LVD is enabled by setting the LVDEN bit, and LVDF bit, which in the Power status register (PMU_CS), indicates if V_{DD} / V_{DDA} is higher or lower than the LVD threshold. This event is internally connected to the EXTI line 16 and can generate an interrupt if it is enabled through the EXTI registers. *Figure 2-4. Waveform of the LVD threshold* shows the relationship between the LVD threshold and the LVD output (LVD interrupt signal depends on EXTI line 16 rising or falling edge configuration). The following figure shows the relationship between the supply voltage and the LVD signal. The hysteresis voltage (V_{hyst}) is 100mV.

LVD application: When the MCU power supply is subject to external interference, such as a voltage drop, we can set the low voltage detection threshold (the threshold is greater than the PDR value) through LVD. Once it falls to this threshold, the LVD interrupt is turned on, which can be used in the interrupt function. Set operations such as soft reset to avoid other exceptions from the MCU.

Figure 2-4. Waveform of the LVD threshold
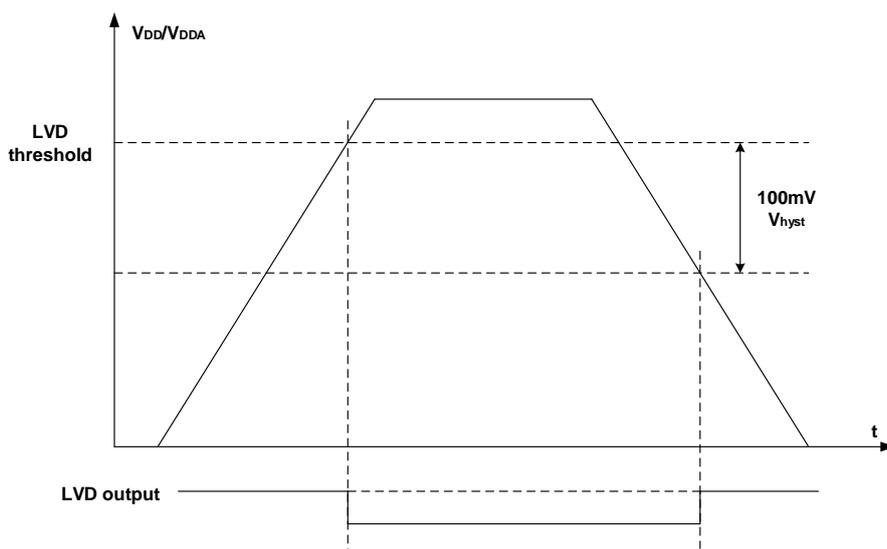
In addition, the MCU reset source can be judged by querying the register RCU_RSTSCK (0x40021024). This register can only clear the flag bit after power-on reset, so during use, after the reset source is obtained, the reset flag can be cleared through the RSTFC control bit. A watchdog reset or other reset event can be more accurately reflected in the RCU_RSTSCK register:

Figure 2-5. RCU_RSTSCK Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LP RSTF	WWDGT RSTF	FWDGT RSTF	SW RSTF	POR RSTF	EP RSTF	OBL RSTF	RSTFC	V12 RSTF				Reserved			
r	r	r	r	r	r	r	rw	r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						Reserved								IRC40K STB	IRC40K EN
														r	rw

The MCU integrates a power-on/power-off reset circuit. When designing an external reset circuit, a capacitor (typical value of 100nF) must be placed on the NRST pin to ensure that the power on the NRST pin generates a low pulse delay of at least 20us, completing effective power-on reset process.
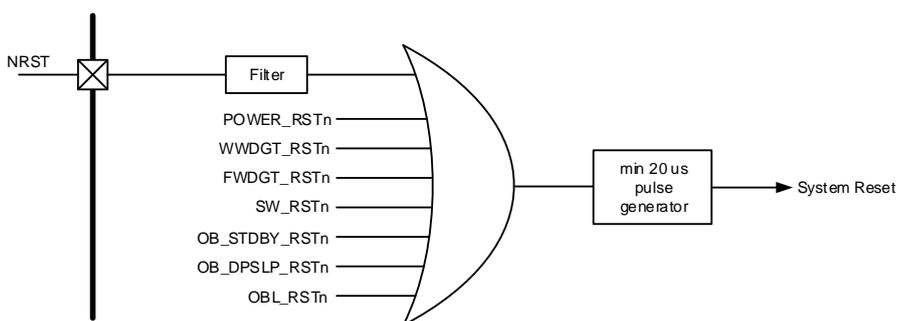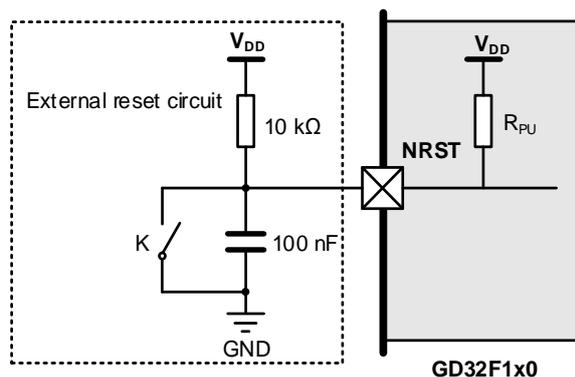
Figure 2-6. System reset circuit

Figure 2-7. Recommended external reset circuit

Note:

1. Internal pull-up resistance R_{PU} = 40 kΩ. You are advised to use an external pull-up resistance of 10 kΩ to ensure that voltage interference does not cause chip abnormalities.
2. If considering the influence of static electricity, an ESD protection diode can be placed at the NRST pin.
3. Although there is a hardware POR circuit inside the MCU, it is still recommended to add an external NRST reset resistor-capacitor circuit.
4. If the MCU starts abnormally (due to voltage fluctuations, etc.), the capacitance value of NRST to ground can be appropriately increased, and extend the MCU reset completion time to avoid the abnormal power-on sequence area.

2.2. Clock

The GD32F1x0 series has a complete clock system inside, and you can choose a suitable clock source according to different applications. The main features of the clock:

■ 3-25MHz external high-speed crystal oscillator (HXTAL) (GD32F130 and GD32F150 products)
■ 14 MHz internal high-speed RC oscillator (IRC8M) (GD32F130 and GD32F150 products)
■ 32.768KHz external low-speed crystal oscillator (LXTAL)
■ 40kHz internal low speed RC oscillator (IRC40K)
■ PLL clock source optional HXTAL or IRC8M
■ HXTAL clock can be monitored

Figure 2-8. Clock tree for GD32F130 and GD32F150 products
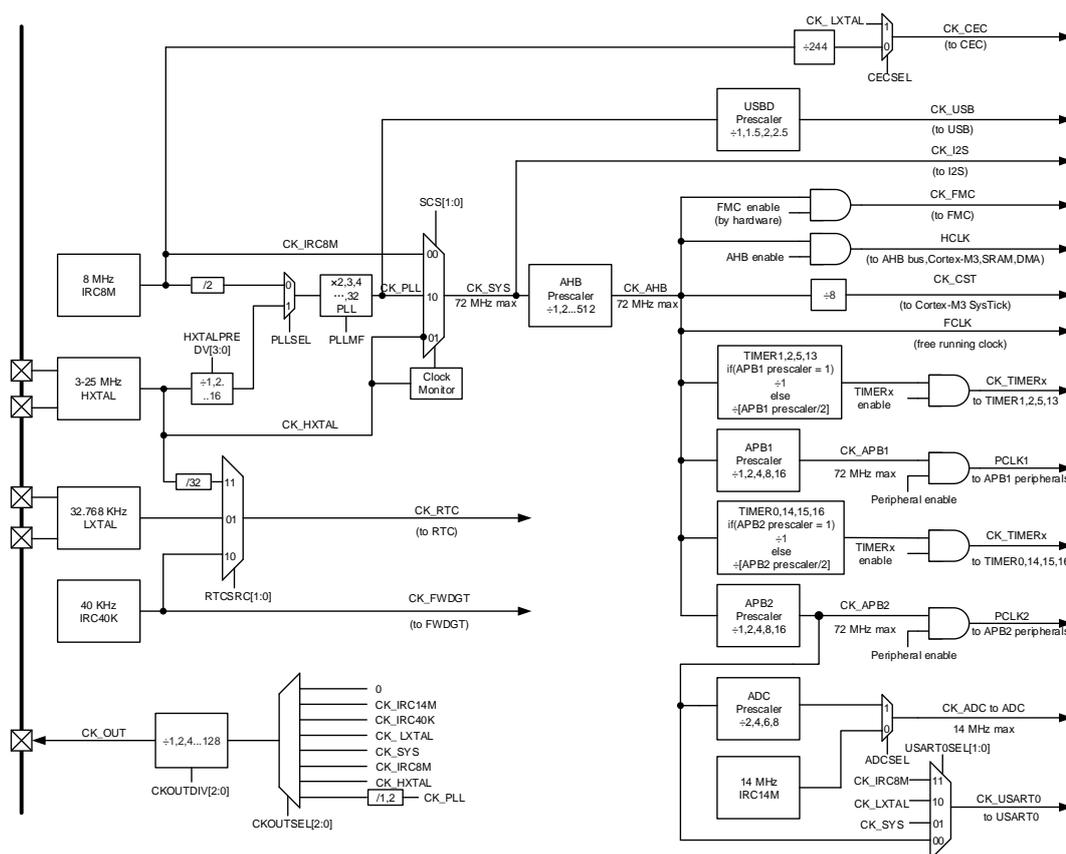
2.2.1. External High-Speed Crystal Oscillator Clock (HXTAL)

The high speed crystal oscillator (HXTAL), produces a highly accurate clock source for use as the system clock. A crystal with a specific frequency must be connected and located close to the two HXTAL pins. The external resistor and capacitor components connected to the crystal are necessary for proper oscillation.

HXTAL can also use the bypass input mode to input the clock source (1-50MHz active crystal oscillator, etc.). When the bypass input is used, the signal is connected to OSCIN, and OSCOUT remains floating. The Bypass function of HXTAL needs to be turned on in software (enable the HXTALBPS bit in RCU_CTL).

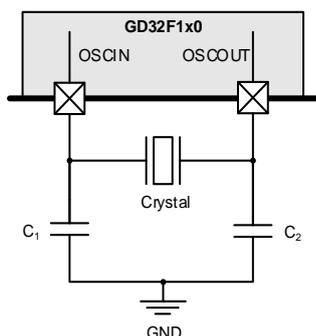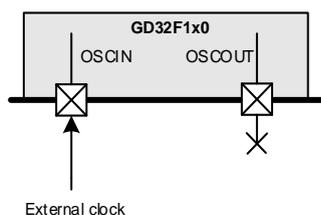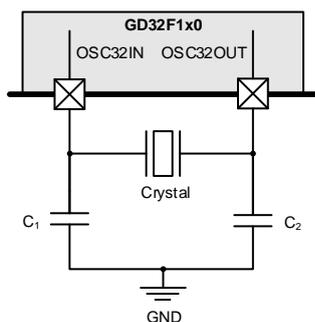**Figure 2-9. HXTAL External crystal circuit**

Figure 2-10. HXTAL External clock circuit

Note：

1. When using the bypass input, the signal is input from OSCIN, and OSCOUT remains floating.

2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, with a typical value of 10pF. When it is recommended to use an external high-speed crystal, try to choose a crystal load capacitance of about 20pF, so that the external matching capacitors C_1 and C_2 can be 20pF, and the PCB layout should be as close to the crystal pin as possible.

3. C_S is the parasitic capacitance on the PCB board traces and IC pins. The closer the crystal is to the MCU, the smaller the C_S, and vice versa. Therefore, in practical applications, when the crystal is far away from the MCU and causes the crystal to work abnormally, the external matching capacitor can be appropriately reduced.

4. When using an external high-speed crystal, it is recommended to connect a 1MΩ resistor in parallel at both ends of the crystal to make the crystal easier to vibrate.

5. Accuracy: external active crystal > external passive crystal > internal IRC8M.

6. When the active crystal oscillator is used normally, Bypass will be turned on. At this time, the high level is required to be no less than 0.7 V_{DD}, and the low level is no more than 0.3 V_{DD}. If Bypass is not turned on, the amplitude requirements of the active crystal oscillator will be greatly reduced.

2.2.2. Low Speed Crystal Oscillator（LXTAL）

The low speed crystal or ceramic resonator oscillator, which has a frequency of 32.768 kHz, produces a low power but highly accurate clock source for the real time clock circuit (Packages below 48 pins do not have LXTAL pins). The RTC module of the MCU is equivalent to a counter, and the accuracy will be affected by the crystal performance, matching capacitance and PCB material. If you want to obtain better accuracy, it is recommended to connect PC13 to the timer input capture pin during circuit design. TIMER to calibrate LXTAL, and set the frequency division register of RTC according to the calibration situation. LXTAL can also support bypass clock input (active crystal oscillator, etc.), which can be enabled by configuring the LXTALBPS bit in RCU_BDCTL.

Figure 2-11. LXTAL External crystal circuit

Figure 2-12. LXTAL External clock circuit
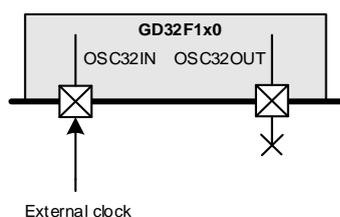
Note:

1. When using the bypass input, the signal is input from OSC32IN, and OSC32OUT remains floating.

2. For the size of the external matching capacitor, please refer to the formula: $C_1 = C_2 = 2*(C_{LOAD} - C_S)$, where C_S is the stray capacitance of the PCB and MCU pins, the empirical value is between 2pF-7pF, and 5pF is recommended as a reference value calculation. When it is recommended to use an external crystal, try to choose a crystal load capacitance of about 10pF, so that the external matching capacitors C_1 and C_2 can be 10pF, and the PCB layout should be as close to the crystal pin as possible.

3. When the RTC selects IRC40K as the clock source and uses the V_{BAT} external independent power supply, if the MCU is powered off at this time, the RTC will stop counting. After the power is re-energized, the RTC will continue to accumulate the counting value according to the previous count value. If the application needs to use V_{BAT} to power the RTC, the RTC can still time normally, and the RTC must select LXTAL as the clock source.

2.2.3. Clock Output Capability (CKOUT)

For GD32F130/GD32F150 series MCU, you can select different clock signal output by configuring the CKOUT0SEL[2:0] bits of the clock register RCU_CFG0. The corresponding GPIO pin PA8 needs to be configured as a multiplexing function to output the selected signal.

Table 2-1. GD32F130/GD32F150 CKOUT0SEL[2:0] Control Bits

Clock source selection bits	Clock source
000	NA
001	CK_IRC14M
010	CK_IRC40K
011	CK_LXTAL
100	CK_SYS
101	CK_IRC8M
110	CK_HXTAL
111	CK_PLL or CK_PLL/2

2.2.4. HXTAL Clock Monitor (CKM)

Set the HXTAL clock monitoring enable bit CKMEN in the clock control register RCU_CTL, HXTAL can enable the clock monitoring function. This function needs to be enabled after HXTAL start-up delay and disabled after HXTAL is stopped. Once the HXTAL fails, the HXTAL will be automatically disabled, and the HXTAL clock blocking flag bit CKMIF in the clock interrupt register RCU_INT is set to generate an HXTAL fault event. The interrupt caused by this fault is connected to the non-maskable interrupt NMI of the Arm® Cortex®-M3.

Note: If HXTAL is selected as the system clock, PLL or RTC clock source, HXTAL failure will prompt the selection of IRC8M as the system clock source, the PLL will be automatically disabled, and the RTC clock source needs to be reconfigured.

2.3. Startup Configuration

The GD32F1x0 series provides three startup modes, which can be selected by the user option byte BOOT1_n bit and BOOT0 pin to determine the startup option. When designing the circuit, run the user program, the BOOT0 pin cannot be left floating, it is recommended to connect a 10kΩ resistor to GND; when running the System Memory to update the program, the BOOT0 pin needs to be connected high, and the option byte OB_USER[4] keeps BOOT1_n at 1 (this When the corresponding BOOT1 bit is 0), after the update is completed, the user program can be run after the BOOT0 is connected to a low level; the SRAM execution program is mostly used in the debugging status.

The embedded Bootloader is stored in the system storage space for reprogramming the FLASH memory. In the GD32F1x0 device, the Bootloader can interact with the outside world through USART0 (PA9 and PA10), USART1 (PA2 and PA3, PA14 and PA15).

Table 2-2. BOOT mode

BOOT mode	BOOT1	BOOT0
Main Flash Memory	X	0
System Memory	0	1
On Chip SRAM	1	1

**Figure 2-13. Recommended BOOT Circuit design**
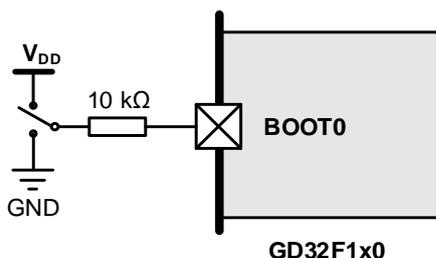
Note: After the MCU is running, if the BOOT state is changed, it will take effect only after the system is reset.

2.4. Typical Peripheral Modules

2.4.1. GPIO Circuit

The GPIO interface supports up to 55 general-purpose input/output ports, and each group of ports provides up to 16 general-purpose input/output pins, which are PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4 ~ PF7, Each pin can be independently configured through registers. The basic structure of the GPIO port is shown in the following figure:

Figure 2-14. Basic structure of a general-purpose I/O
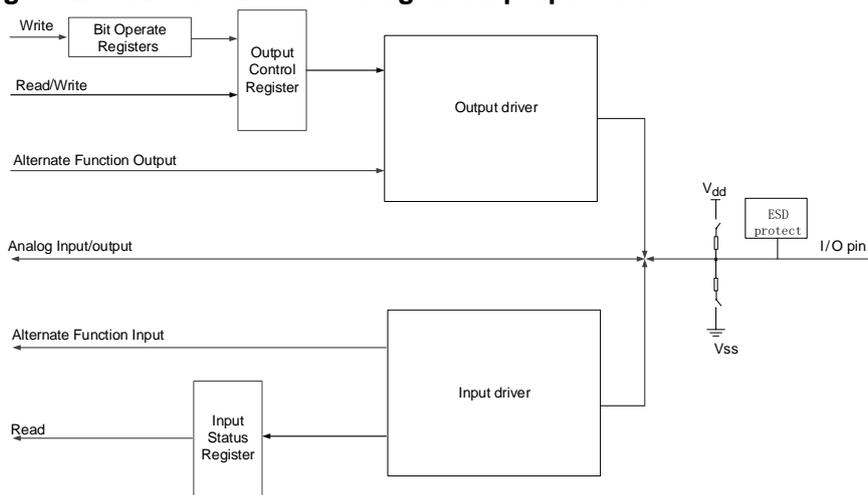
Note:

1. The IO port is divided into 5V tolerance and non-5V tolerance. When using, pay attention to distinguish the voltage tolerance of the IO port, see Datasheet for details.

2. When the 5V-tolerant IO port is directly connected to 5V, it is recommended that the IO port be configured in open-drain mode and externally pull up to work.

3. After the IO port is powered on and reset, the default mode is floating input, and the level characteristics are uncertain. In order to obtain more consistent power consumption, it is recommended that all IO ports be configured as analog inputs and then modified to the

corresponding mode according to application requirements (chip Ports that are not exported internally also need to be configured).

4. To improve EMC performance, it is recommended to pull up or pull down the unused IO pins by hardware.

5. The three IO ports of PC13, PC14, and PC15 have weak drive capability and limited output current capability (about 3mA). When configured in output mode, their operating speed cannot exceed 2MHz (maximum load is 30pF).

6. The same label PIN in multiple groups can configure only one IO port as an external interrupt. For example, PA0, PB0, and PC0 only support one of the three IO ports to generate external interrupts, and do not support three external interrupt modes.

7. Non-5V tolerance I/O, external voltage over V_{DD}, may generate perfusion current.

2.4.2. ADC Circuit

GD32F1x0 series integrates a 12-bit SAR ADC, it has up to 19 channels, can measure 16 external and 2 internal signal sources and 1 external battery monitoring signal source. The internal signal is the temperature sensor channel (ADC0_IN16), the internal reference voltage input channel (ADC0_IN17), and the external signal is the external monitoring battery V_{BAT} power supply pin input channel (ADC0_IN18). The temperature sensor reflects the change in temperature and is not suitable for measuring absolute temperature. If accurate temperature measurement is required, an external temperature sensor must be used. The internal reference voltage V_{REFINT} provides a regulated voltage output (1.2V) to the ADC and is internally connected to ADC0_IN17. Provides the function of externally detecting the battery voltage of the V_{BAT} pin, and the converted value is $V_{BAT}/2$.

If the ADC collects the external input voltage during use, if the sampled data fluctuates greatly, it may be due to the interference caused by power supply fluctuations. You can calibrate by sampling internal V_{REFINT} and then calculate the externally sampled voltage.

When designing the ADC circuit, it is recommended to place a small capacitor at the ADC input pin, and it is recommended to place a small capacitor of 500pF.

Figure 2-15. ADC Acquisition Circuit Design
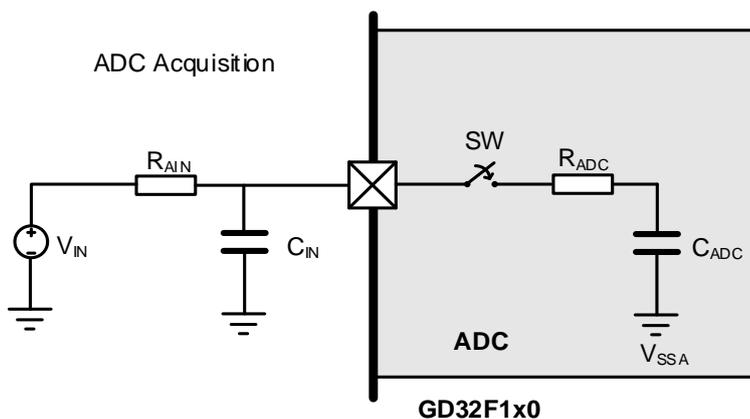
When f_{ADC} = 14MHz of the GD32F130/GD32F150 series MCU, the relationship between the

input impedance and the sampling period is as follows. In order to obtain better conversion results, it is recommended to reduce the frequency of f_{ADC} as much as possible during use, and select a larger value for the sampling period. When designing external circuits, try to reduce the input Impedance, if necessary, use the op amp to follow to reduce the input impedance.

Table 2-3. f_{ADC} =14MHz Relationship between sampling period and external input impedance

T_s(cycles)	t_s(us)	R_{AINmax} (kΩ)
1.5	0.11	0.14
7.5	0.54	1.5
13.5	0.96	2.9
28.5	2.04	6.3
41.5	2.96	9.3
55.5	3.96	12.5
71.5	5.11	16.2
239.5	17.11	54.8

2.4.3. DAC Circuit

GD32F150 series has a DAC inside, which can convert 12-bit digital data to voltage output on external pins. Data can be in 8-bit or 12-bit mode, left-justified or right-justified. When external triggering is enabled, DMA can be used to update digital data on the input. At the output voltage, the DAC output buffer can be used to obtain higher drive capability.

Table 2-4. DAC Related Pin Description

Name	Notes	Signal Type
V_{DDA}	Analog power	Input, Analog power
V_{SSA}	Analog power ground	Input, Analog power ground
DAC_OUT	DAC Analog output	Analog output signal

Before enabling the DAC module, the GPIO port should be configured in analog mode.

For GD32F150 products, there is only one DAC with PA4.

2.4.4. USB Circuit

The GD32F150 series MCU has a built-in USB interface, which is a USBFS module. The USB protocol requires a clock accuracy of not less than 500ppm, and the internal clock may not be able to achieve such accuracy, so it is recommended to use an external crystal or an active crystal oscillator as the USB module clock source when using the USB function.

GD32F150 series USB can only be designed as USB device, and the DP line needs an external 1.5K pull-up resistor.

When designing the circuit, in order to improve the ESD performance of the USB, it is

recommended to design a resistance-capacitance discharge isolation circuit for the USB case.

**Figure 2-16. Recommend USB-Device Reference Circuit**
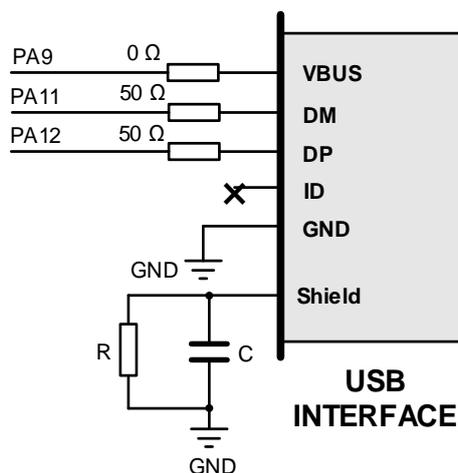
Recommendation: R = 1MΩ, C = 4700pF

2.4.5.   Standby mode wake-up circuit

GD32F1x0 series supports three low-power modes, namely sleep mode, deep-sleep mode and standby mode. The standby mode with the lowest power consumption is the standby mode, which requires the longest wake-up time. Wake-up from Standby mode can be woken up by the rising edge of the WKUP pin. At this time, there is no need to configure the corresponding GPIO, just configure the WUPENx bit in the PMU_CS register. There are 2 WKUP wake-up pins in total. The reference circuit is designed as follows:

Figure 2-17. Recommend Standby external Wake-up pin circuit design
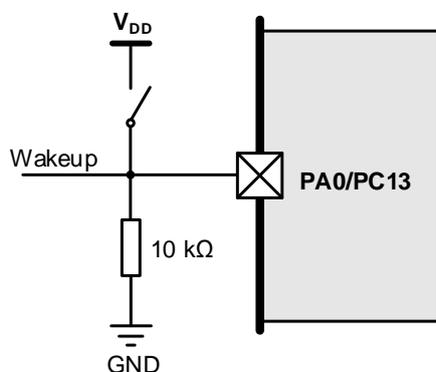
Note: In this mode, should pay attention to the circuit design. If there is a series resistance between the WKUP pin and V_{DD}, additional power consumption may be added.

2.5. Download the debug circuit

GD32F1x0 series cores only support SWD debug interface, not JTAG interface. The SWD interface standard is a 5-pin interface, of which 2 are signal interfaces.

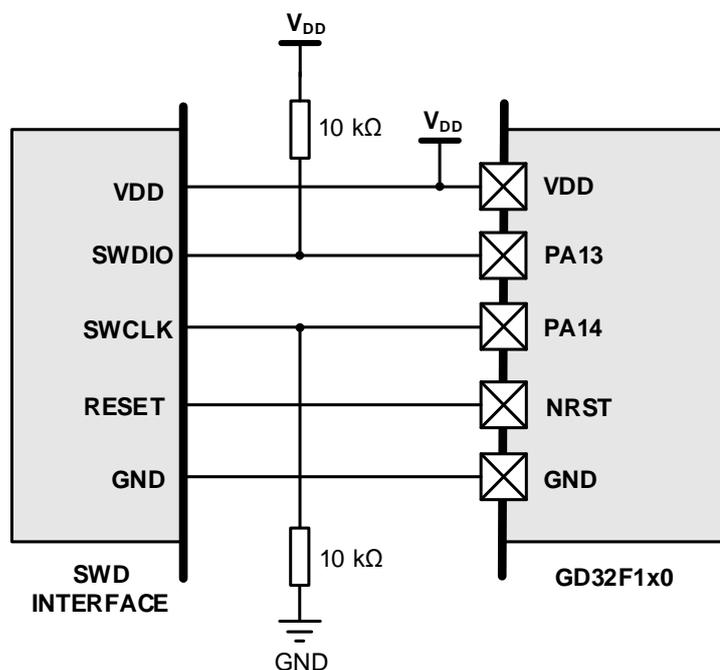**Note:** After reset, the debug related ports are in input PU/PD mode, where:

PA13：SWDIO is in pull-up mode.
PA14：SWCLK is in pull-down mode.

Table 2-5. SWD Download debug interface assignment

Alternate function	GPIO Port
SWDIO	PA13
SWCLK	PA14

**Figure 2-18. Recommend SWD Wiring Reference Design**

There are several ways to improve the reliability of SWD download and debugging communication and enhance the anti-interference ability of download and debugging.

1. Shorten the length of the two SWD signal lines, preferably within 15cm.
2. Weave the two SWD wires and the GND wire into a twist and twist them together.
3. Connect separately tens of pF small capacitors in parallel between the two signal lines of the SWD and the ground.
4. Any IO of the two signal lines of SWD is connected in series with a 100Ω~1KΩ resistor.

2.6. Reference Schematic Design

**Figure 2-19. GD32F1x0 Recommend reference schematic design**
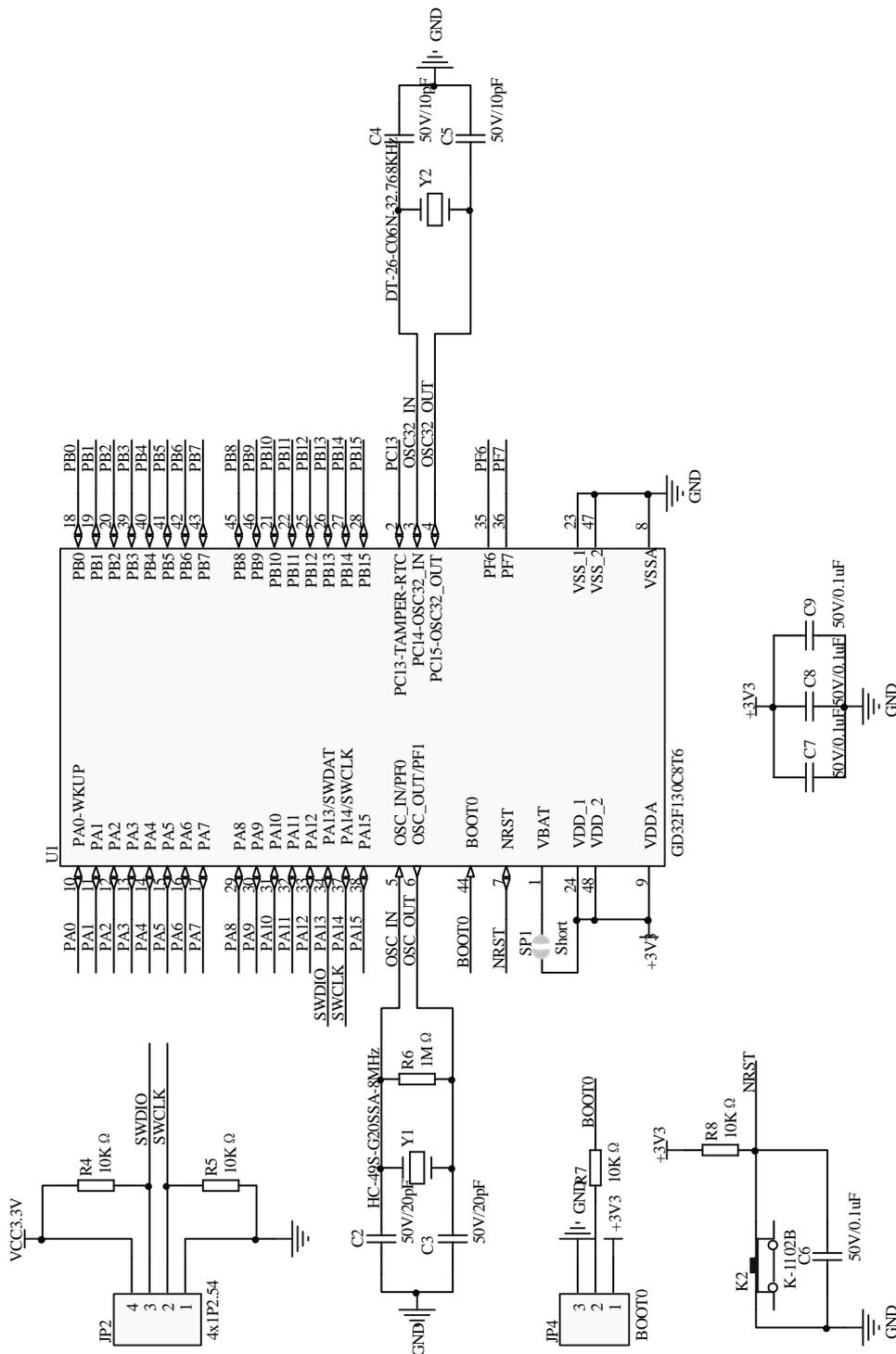
3.   PCB Layout design

In order to enhance the functional stability and EMC performance of the MCU, it is not only necessary to consider the performance of the supporting peripheral components, but also the PCB Layout. In addition, when conditions permit, try to choose a PCB design solution with an independent GND layer and an independent power supply layer, which can provide better EMC performance. If conditions do not allow, independent GND layer and power supply layer cannot be provided, then it is also necessary to ensure a good power supply and grounding design, such as making the GND plane under the MCU as complete as possible.

3.1.   Power supply decoupling capacitors

The GD32F1x0 series power supply has three power supply pins: V_{DD}, V_{DDA} and V_{BAT}. The 100nF decoupling capacitor can be made of ceramic, and it is necessary to ensure that the position is as close to the power supply pin as possible. The power trace should try to make it pass through the capacitor first and then reach the MCU power pin, It is recommended to punch holes near the capacitor pad to connect with GND.

Figure 3-1. Recommend Power Pin Decoupling Layout Design
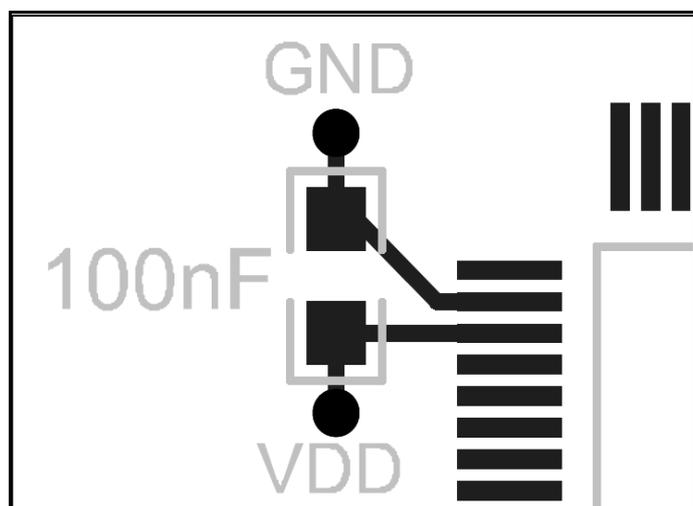
3.2.   Clock Circuit

GD32F1x0 series clocks have HXTAL and LXTAL, and the clock circuit (including crystal or crystal oscillator and capacitor, etc.) is required to be placed close to the MCU clock pin, and the clock trace should be wrapped by GND as much as possible.

**Figure 3-2. Recommend Clock Pin Layout Design (passive crystal)**
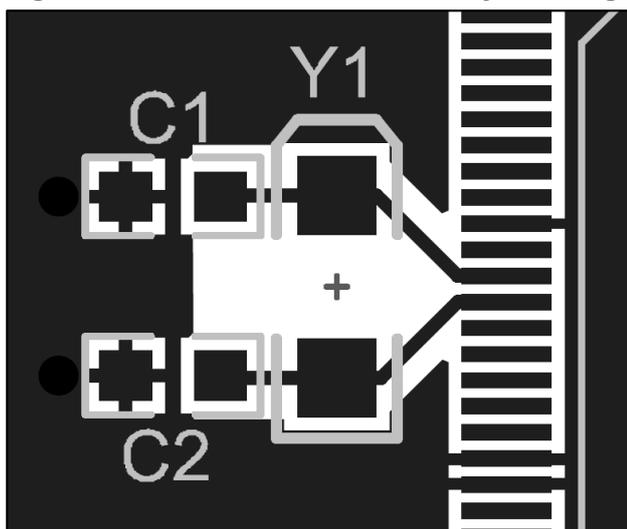
Note:

1. The crystal should be as close to the MCU clock pin as possible, and the matching capacitor should be as close as possible to the crystal.
2. The whole circuit should be on the same layer as the MCU, and the wiring should not go through the layer as much as possible.
3. High-power, high-interference risk devices and high-speed wiring should be kept away from the clock crystal circuit as far as possible.
4. The clock line performs packet ground processing to achieve shielding effect.

3.3.   Reset Circuit

NRST trace PCB Layout reference is as follows:

Figure 3-3. Recommend NRST Trace Layout Design
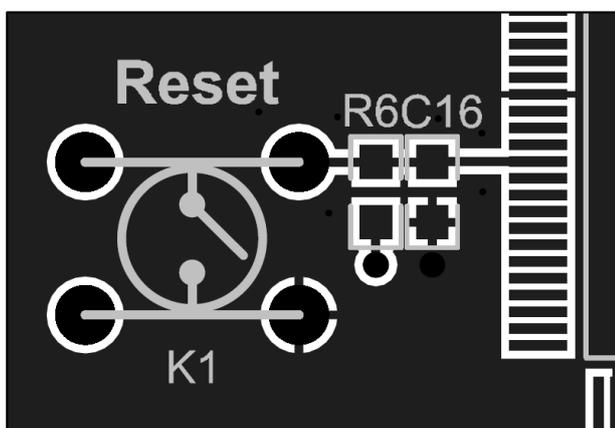
Note: The resistance and capacitance of the reset circuit should be as close as possible to the NRST pin of the MCU, and the NRST trace should be kept away from devices with strong interference risk and high-speed traces as far as possible. If conditions permit, it had better

to wrap the NRST traces for better shielding effect.

3.4.   USB Circuit

USB module has two differential signal lines, DM and DP. It is recommended that the PCB traces require a characteristic impedance of 90ohm. The differential traces should be run in strict accordance with the rule of equal length and equal distance, and try to keep the traces as short as possible. If the two differential lines are not equal in length , the short line can be compensated with a serpentine line at the terminal.

Due to impedance matching considerations, the series matching resistance is recommended to be about 50Ω. When the USB terminal interface is far away from the MCU, the series resistance value needs to be appropriately increased.

USB differential trace reference is as follows:

Figure 3-4. Recommend USB Differential Trace Layout Design
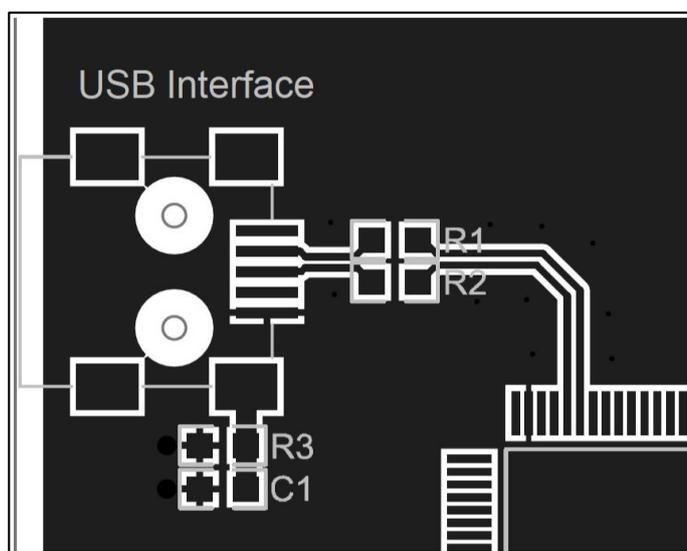
Recommendation：R1 = R2 = 50Ω, R3 = 1MΩ, C = 4700pF

Note：

1. Reasonable placement during layout to shorten the differential trace distance.
2. Draw differential lines first, try not to exceed two pairs of vias for a pair of differential lines, and place them symmetrically.
3. Symmetrical parallel wiring to ensure that the two lines are tightly coupled, avoiding 90°, arc or 45° wiring.
4. Devices such as resistance-capacitor, EMC connected to the differential traces, or test points should also be symmetrical.

4.   Package description

GD32F130 series has a total of 6 package types, TSSOP20, QFN28, QFN32, LQFP32, LQFP48 and LQFP64.

GD32F150 series has a total of 4 package types, QFN28, QFN32, LQFP48 and LQFP64.

Table 4-1. Package Part Number Description

Part Number	Package
GD32F130FxP6	TSSOP20(6.5x4.4, 0.65 pitch)
GD32F130GxU6/GD32F150GxU6	QFN28(4x4, 0.4 pitch)
GD32F130KxU6/GD32F150KxU6	QFN32(5x5, 0.5 pitch)
GD32F130KxT6	LQFP32(7x7, 0.8 pitch)
GD32F1x0CxT6	LQFP48(7x7, 0.5 pitch)
GD32F1x0RxT6	LQFP64(10x10, 0.5 pitch)

(Original dimensions are in millimeters)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Apr.7, 2023

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