GigaDevice Semiconductor Inc.

Guidelines for Radio Frequency Hardware Development of GD32VW553 Series

Application Note
AN148

Revision 1.1

(Mar.2024)

Table of Contents

List of Figures

List of Tables

1. Foreword

This guideline is intended for developers of 32-bit universal MCU GD32VW553 series of RISC-V-based highly-integrated 2.4GHz Wi-Fi6 + BLE system on chip (SOC). It gives a general introduction to development of hardware of GD32VW553 series, like power supply, resetting, clock and RF circuits. The purpose of the Application Notes is to enable developers to quickly get started with GD32VW553, quickly develop and use the product hardware, and save time for studying the manual, thus accelerating the product development progress.

The Application Notes is described in six parts:

1. Power supply: It mainly introduces the design of the power management, and power supply of GD32VW553 series.
2. Resetting: It mainly introduces the design of resetting function and mode selection of GD32VW553 series.
3. Radio frequency: It mainly introduces the design of RF circuits of GD32VW553 series.
4. Clock: It mainly introduces the design of the high and low speed clock functions of GD32VW553.
5. Reference circuit and PCB layout design: It mainly introduces the precautions for hardware circuit design and PCB layout design of GD32VW553 series.
6. Package description: It mainly introduces the types and names of packages included in GD32VW553.

This document also introduces the minimum system hardware resources used in GD32VW553 application development.

Table 1-1. Applicable product

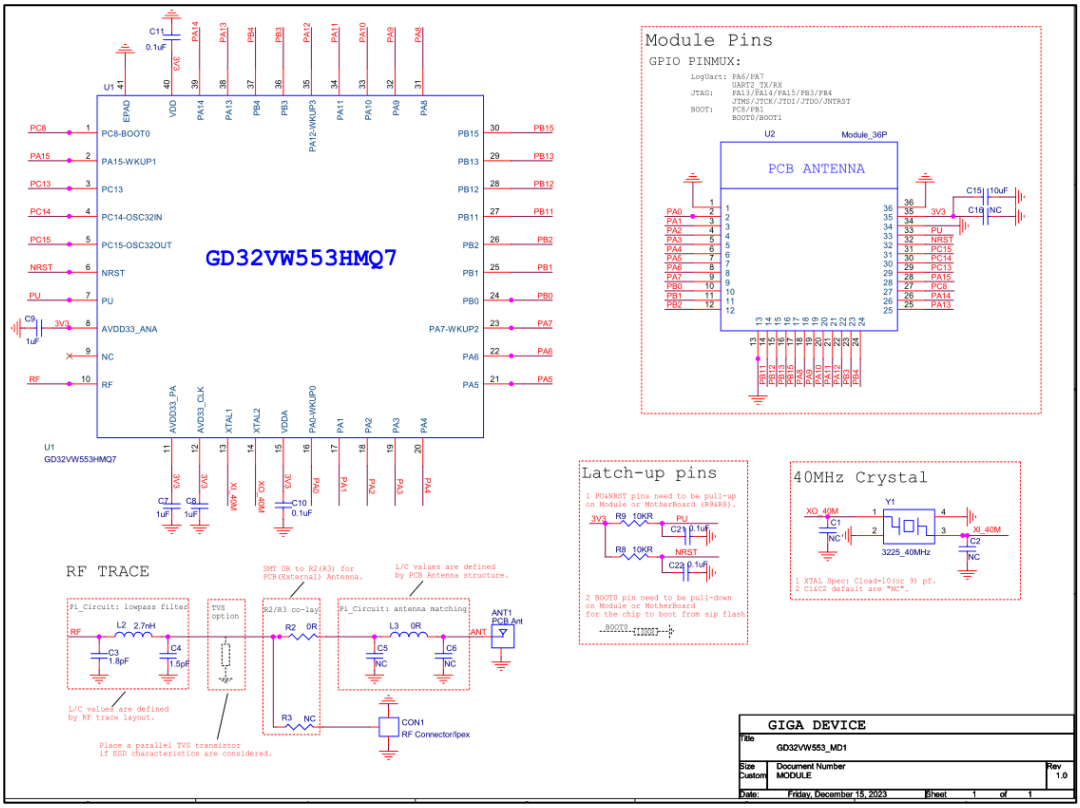
Type	Model
MCU	GD32VW553 Series

2. Hardware design

The schematic diagram of reference design of MCU module of GD32VW553 series is shown as ***Figure 2-1. Circuit diagram of MCU module of GD32VW553 series*** **(taking version HMQ7 as an example)**. Pay attention to the following items in the schematic diagram design:

- Circuit design for power supply
- Circuit design for resetting and mode selection
- RF circuit design
- XTAL circuit design
- LXTAL circuit design

Figure 2-1. Circuit diagram of MCU module of GD32VW553 series



2.1. Circuit design for power supply

Power supply pins of MCU module of GD32VW553 series include two types: power supply pins for the MCU RF part and for the MCU digital and analog part. The former includes RF VCO power supply AVDD33_ANA (Pin8), RF PA&LNA power supply AVDD33_PA (Pin11), and RF XTAL power supply AVDD33_CLK (Pin12). The latter includes the MCU analog power supply pin VDDA (Pin15) and the MCU and Wi-Fi digital power supply pin VDD (Pin40). The standard working voltage of all power supply pins above is 3.3 V.

It is recommended to place two capacitors (one large and one small) at the entrance of the

module's power supply (as shown in ***Figure 2-2. Circuit at the entrance of module power supply***. Only the large capacitor is placed by default (like 10 uF). At the same time, filter capacitors are placed individually at each power supply pin. It is recommended to use 1 uF filter capacitors for RF power supply pins like AVDD33_ANA, AVDD33_PA, and AVDD33_CLK (as shown in ***Figure 2-3. Circuit of RF power supply pins of the chip***. For other power supply pins like VDDA and VDD, it is accepted to use 0.1 uF filter capacitors (as shown in ***Figure 2-4. Circuit of other power supply pins of the Chip***.

Figure 2-2. Circuit at the entrance of module power supply

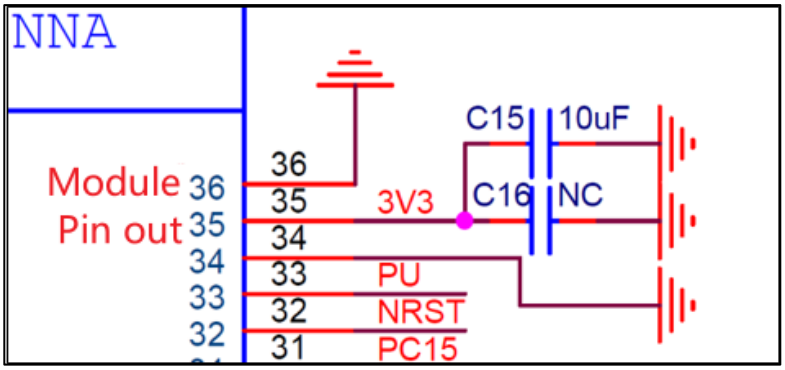
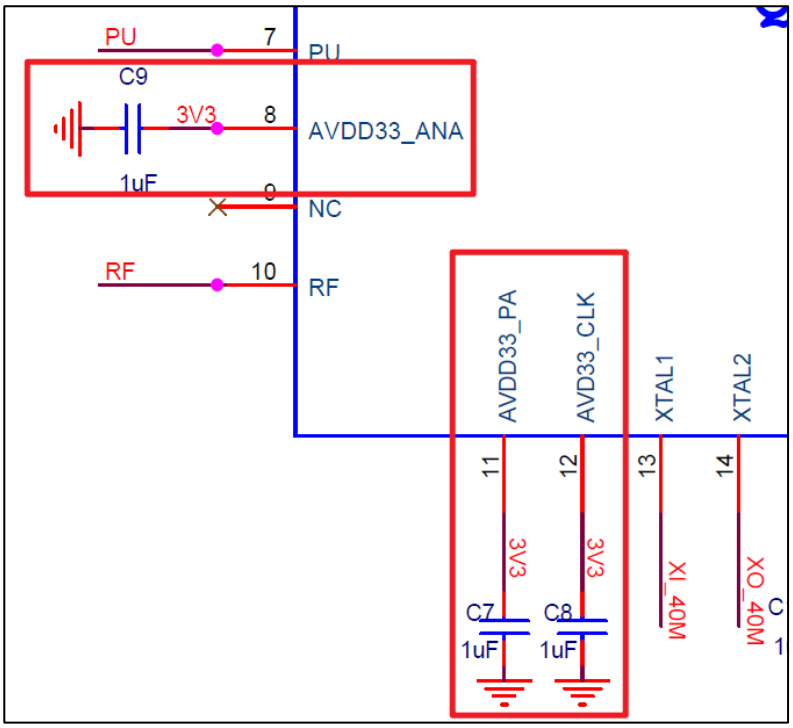
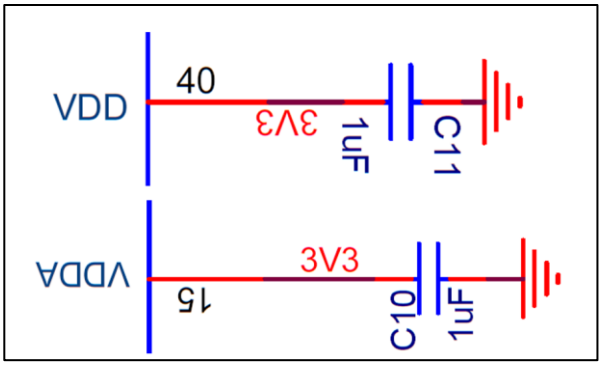


Figure 2-3. Circuit of RF power supply pins of the chip



When the WiFi or BLE function of GD32VW553 is not used, AVDD33_CLK supplies power normally and a 1 uF decoupling capacitor is installed. It is recommended that AVDD33_PA and AVDD33_ANA should supply power, but decoupling capacitor may not be installed to save BOM.

Figure 2-4. Circuit of other power supply pins of the Chip



2.2. Circuit design for resetting and mode selection

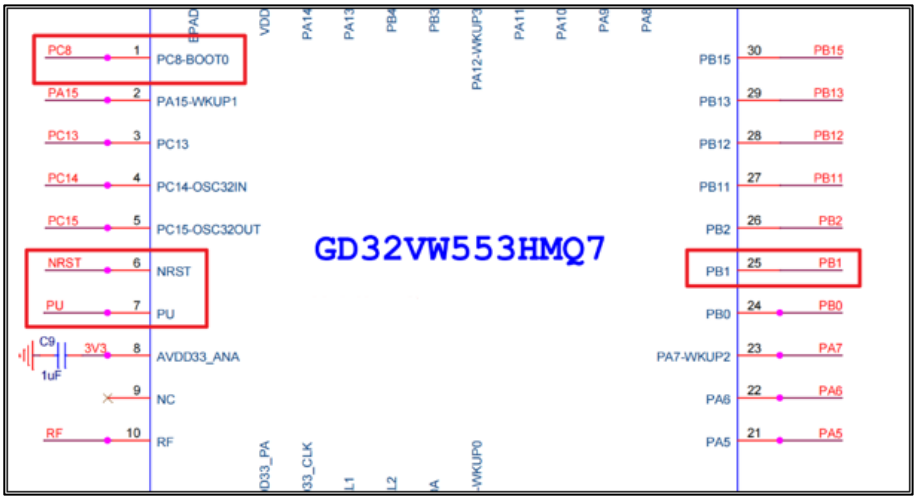
GD32VW553 pins PU (Pin7) and NRST (Pin6) are chip power supply enable and reset pins respectively. The chip can operate only when both are pulled up. A filter capacitor and a pull-up resistor can be placed near the pins in the design. If a bottom board is used, a pull-up resistor and a filter capacitor can also be placed on the bottom board. In actual use, only one is required to be selected as the enable pin while the other one still needs to be connected with pull-up resistor and filter capacitor. If GD32VW553 is used as the master MCU, it is recommended to use NRST as the enable pin and always pull up PU. If GD32VW553 is used as the slave device, it is recommended to use PU as the enable pin and always pull up NRST.

The selected pins for the boot mode of GD32VW553 are BOOT0 (Pin1) and BOOT1 (Pin25). Definitions of several modes are shown in ***Table 2-1. BOOT mode***. It is generally recommended to place the pull-up or pull-down resistor on the bottom board. If it is used for a single module, it is required to reserve a pull-up or pull-down resistor on the module. Reference design is as shown in ***Figure 2-5. Circuit for resetting and mode selection*** where pull-up and pull-down resistors are placed on the bottom board.

Table 2-1. BOOT mode

BOOT1	BOOT0	Start-up Mode
x	0	Flash
0	1	Legacy Bootloader
1	1	SRAM

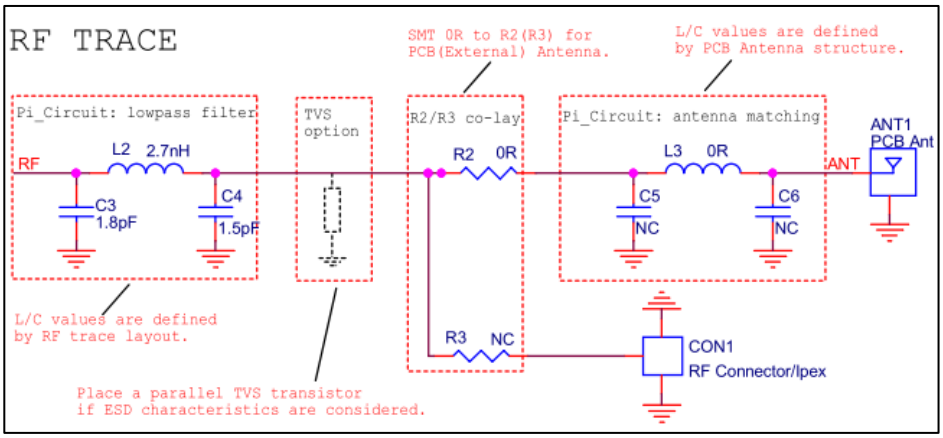
Figure 2-5. Circuit for resetting and mode selection



2.3. RF circuit design

GD32VW553 RF circuit reference design is as shown in ***Figure 2-6. RF circuit***. RF pin of the chip is Pin10. In the path, there is one group of π-type (CLC combination) matching circuits which are mainly used to filter higher harmonics of radio frequency transmission signal (to meet certification requirements) and fit for impedance matching debugging. Both capacitors and inductors in the matching circuit are required to use materials in compliance with RF specifications with precision of ±0.1 pF (nH). By default, specification of the component combination of the matching circuit is 1.8 pF + 2.7 nH + 1.5 pF. The final specification is subject to actual debugging result of different PCBs. When matching components are not added, the default is series components. 0R resistors are recommended and parallel components are NC. For antenna, developers can use PCB antenna or external antenna. It is recommended to reserve RF test connector to conduct conduction test and external antenna test. In addition, it is required to reserve π-type network for antenna matching. Place a parallel TVS transistor between two π-type network if ESD characteristics are considered.

Figure 2-6. RF circuit



2.4. XTAL circuit design

GD32VW553 module supports patch passive transistors at frequencies like 40 MHz and 26 Mhz. 40 MHz is used by default. 3225, 2520 and other options are available for packaging. The transistor circuit of MCU of GD32VW553 series is shown in ***Figure 2-7. Transistor circuit***. The two load capacitors are normal close (NC). Frequency offset is corrected by adjusting internal capacitors of the chip. In consideration of load capacitor NC, the load capacitance index of the transistor is required to be 10 pF (or 9 pF) (see "Load Capacitance" in ***Figure 2-8. Recommended transistor indexes***). For other index requirements, please refer to the contents in the red box.

Figure 2-7. Transistor circuit

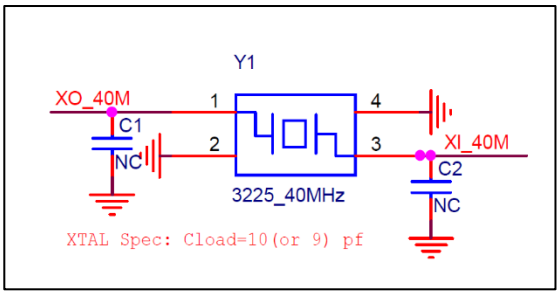


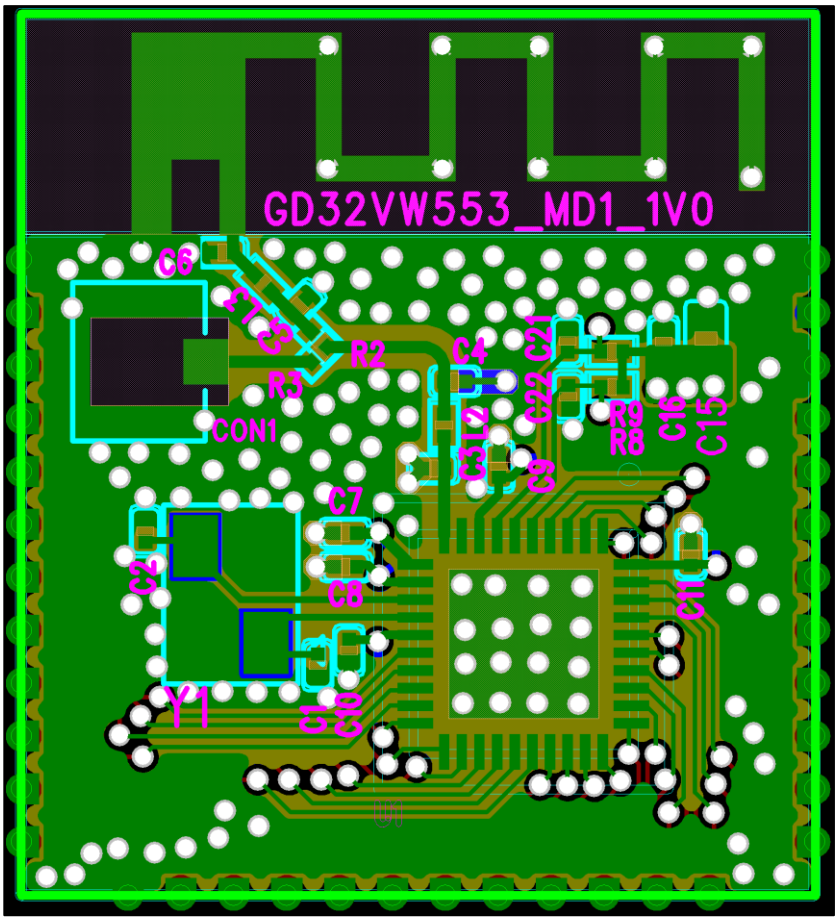
Figure 2-8. Recommended transistor indexes

	Parameters	SYM.	Electrical Spec.				Notes
			MIN	TYPE	MAX	UNITS	
1	Nominal Frequency	FL		40.000000		MHz	-
2	Oscillation Mode	-		Fundamental		-	-
3	Load Capacitance	CL		10		pF	-
4	Frequency Tolerance	-		±10		ppm	at 25 ℃ ± 3 ℃
5	Frequency Stability	-		±10		ppm	Over Operating Temp. Range (Reference 25℃)
6	Operating Temperature	-	-30	~	85	℃	-
7	Aging	-		±3		ppm	1st Year
8	Drive Level	DL	-	100	500	μW	-
9	Effective Resistance Rr	Rr	-	-	30	Ω	-
10	Shunt Capacitance C0	C0	-	-	3	pF	-
11	DLD2	-	-	-	10	Ohms	-
12	FDLD	-	-	-	10	ppm	-
13	SPDB	-	-	-	-3	dB	-
14	Insulation Resistance	-	500	-	-	MΩ	at DC 100V
15	Storage Temperature Range	-	-40	~	85	℃	-

3. PCB Layout design

Layout of the reference design of GD32VW553 module is as shown in *Figure 3-1. GD32VW553 module layout*.

Figure 3-1. GD32VW553 module layout



Pay attention to the following items in the layout design of GD32VW553 module:

- PCB stack-up design
- Circuit design for power supply
- RF circuit design
- XTAL circuit design
- GND integrity and EPAD design
- Shielding case design
- Routing and copper pour design

3.1. PCB stack-up design

PCB stack-up of GD32VW553 module must be designed to use a four-layer board. For definition of layer, please refer to *Table 3-1. Reference definition of PCB layer*:

Table 3-1. Reference definition of PCB layer

Number of Board Layers	Four-Layer Board
Reference definition of layer	Layer 1: SMD & Signal & VCC Layer 2: GND Layer3: VCC Layer 4: GND & (Signal/VCC)

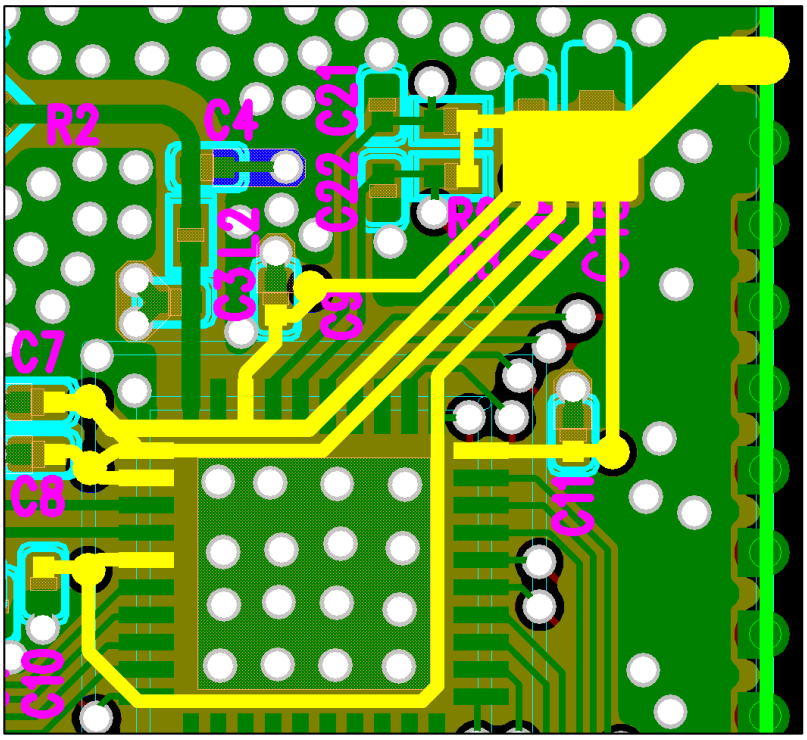
Ensure that layer 2 is of complete GND, and minimize routing for power supply and sensitive signal of bottom layer (in consideration of bottom layer EMI) in the design.

3.2. Circuit design for power supply

Routing of 3.3 V power supply is recommended to use the "star-shaped" power supply mode as shown in the yellow highlighted part of ***Figure 3-2. Circuit layout design for power supply***. Each power supply pin is individually routed from the 3.3 V power supply to the chip pin. A large capacitor is placed at the 3.3 V power supply. A copper plane can also be used at the power supply. Width of routing for the end from the 3.3 V power supply to the module is recommended to be 20 to 30 mil. For branch routing, width of routing of PA power supply pin (Pin11) should be at least 10 mil and width of routing of other power supply pins can be 6 to 8 mil.

Routing of 3.3 V power supply should be on VCC layer (layer3) as much as possible. Power supply cable of top layer should be installed inside the shielding case and away from the board edge. Routing of power supply should not in parallel with the high-speed signal wires. At signal intersection of adjacent layers, the routing should be vertical. Routing of each power supply pin should pass through the filter capacitor and then connect to the pin. The capacitor should be placed as close to the pin as possible. Holes (1 to 2 vias) of the capacitor GND pad is drilled down to the ground and the capacitors should not share GND vias. Holes of GND pads of filter capacitors of sensitive pins (like AVD33_ANA, AVDD33_PA, and AVDD33_CLK) should be drilled individually in the clearance area on the TOP layer to GND copper pour of Layer 2, 3 or 4 and should not connected to TOP GND copper pour.

Figure 3-2. Circuit layout design for power supply



3.3. RF circuit design

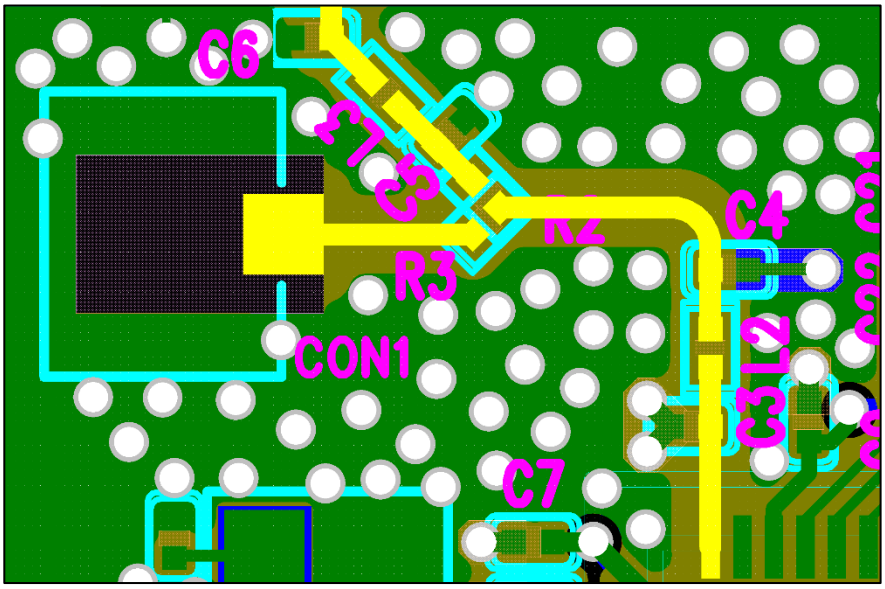
RF routing impedance should remain 50 ohm. In the design, routing width and distance should be measured according to dielectric constant of plates, PCB stacked structure, and other information to ensure consistent impedance for RF routing and avoid sudden change or offset of impedance. In consideration of errors due to process precision and other factors at plate-making, it is recommended to be at least 10 mil wide for RF routing.

As shown in ***Figure 3-3. RF circuit layout design***, RF routing should be as short as possible to ensure the layer below is a complete GND (unlimited transmission routing) and avoid entry into any other layers and bending. When bending is required, the angle should be larger than 90° and the routing should be curved. The routing should be away from any power supply cable and high-speed signal cable to avoid coupling of strong RF signals and interference with other components. On the two sides of the routing, two rows of GND vias are placed at a minimum interval for shielding. For some places where branching is required, the 0R resistor co-lay mode can be used (R2 and R3 in the figure).

Third-order Π-type network should be as close to RF Pin as possible and placed in Z shape. The GND pad of capacitor C3 at the near end of RF PIN should be connected to GND through two vias against the pad in the clearance area on the TOP layer and a clearance area on the TOP layer is added to make it not connected to TOP GND copper pour. The GND pad of capacitor C4 at the far end should have one stub in the clearance area on the TOP layer and be then connected to GND through the vias. GND layer (Layer 2) should have the same clearance area (in other words, the stub should use the ground of VCC layer for reference

and the vias are only connected to GND copper pour of Layer 3 or 4). The total length of the stub plus the vias from TOP layer to VCC layer should be about 55 mil. The stub plus the longer grounding vias can be equivalent to a strong inductor. Two parallel short grounding vias can be equivalent to a weak inductor. In this case, the matching circuit structure can be equivalent to (C+L)+L+(C+L). The purpose of the above-mentioned means is to build an asymmetry in the matching circuit structure to easily filter out second-order and third-order harmonics and tune impedance matching at a smaller grounding capacitance, reducing the passband interpolation loss of the matching circuit.

Figure 3-3. RF circuit layout design



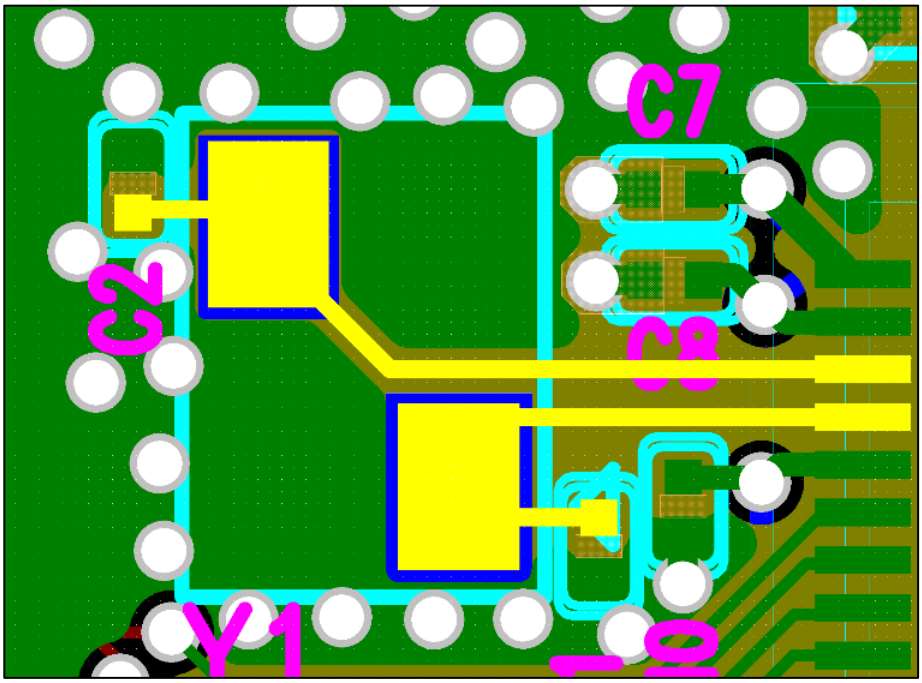
As shown in ***Figure 3-4. PCB antenna design***, PCB antenna is required to be placed near the board edge, away from other transmission wires and components (particularly transmission wires or components for high-frequency signals) and isolated from any external circuit with one to two rows of GND vias (at a minimum interval). In the antenna area, all PCB layers are required to be cleared (namely no copper pour). It is recommended that no window should be open on the Solder mask Top layer (Solder mask should be used to protect the antenna copper plate).

Figure 3-4. PCB antenna design

3.4. XTAL circuit design

As shown in ***Figure 3-5. Transistor circuit design***, the transistor should be as close to the chip pin (XI&XO) as possible, away from magnetic induction components (like power inductors) and radiation components (like antenna) and isolated from other signal routes on the same layer with GND copper pour and vias. The width of the input and output lines (XI&XO) of the transistor can be 6 mil. The routing should be as short as possible and have less bending. The routing can't be cross layers or cross over each other. The load capacitors on both sides can be connected to respective GND pads of the transistor and multiple GND vias can be placed to improve heat dissipation. Transmission routing should be minimized beneath the transistor to maintain complete GND copper pour.

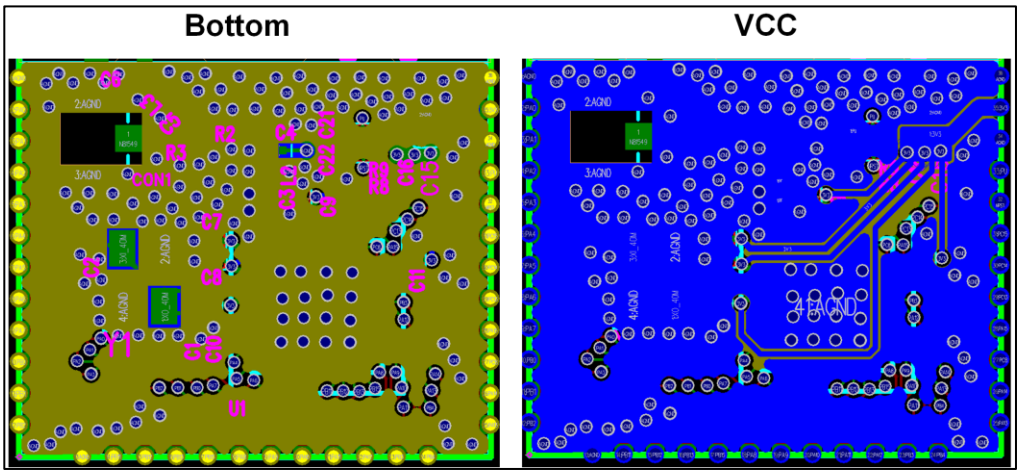
Figure 3-5. Transistor circuit design



3.5. GND integrity and EPAD design

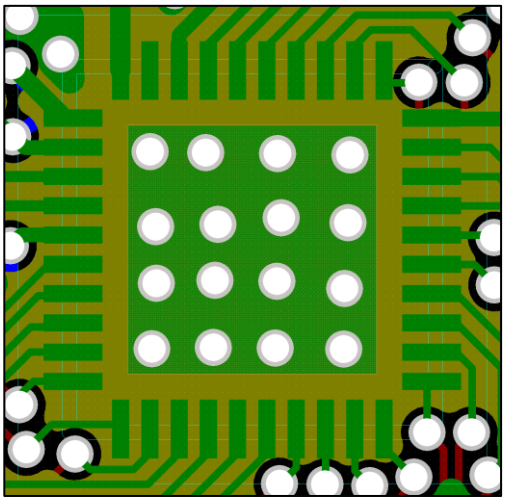
Layer 2 (GND layer) should be a complete GND Plane to ensure that RF, XTAL and other parts on the TOP layer are not affected. At the same time, attention should be paid to the integrity of GND copper pour on the VCC and Bottom layers to avoid "isolation" as shown in ***Figure 3-6. GND integrity design on the VCC and bottom layers***.

Figure 3-6. GND integrity design on the VCC and bottom layers



For chip EPAD, it is recommended not to connect to external copper pour on the TOP layer. More GND vias can be drilled to facilitate heat dissipation, as shown in *Figure 3-7. Chip EPAD design*.

Figure 3-7. Chip EPAD design



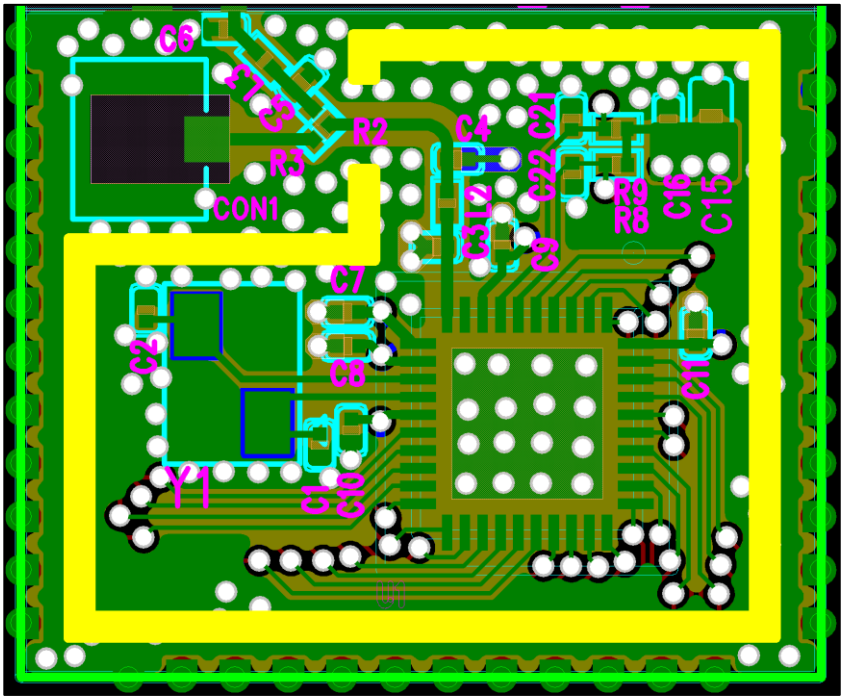
3.6. Shielding case design

All components and routes of the TOP layer of the module should be limited in the shielding case as much as possible. For routes (like RF routes) that need to be out from the shielding case on the TOP layer, the shielding case should have "wiring hole". Other routes can be on the Bottom or VCC layer.

The width of the border of the shielding case should be at least 24 mil. More GND vias can be placed at the pad of the border. The distance between the shielding case and the pad on the edge of the board & the routing should be at least 15 & 10 mil respectively. The height of the shielding case depends on the height of components. When designing antenna, the effect of the height of the shielding case should also be considered. The reference design of the pad of the shielding case is shown by the yellow highlighted part in *Figure 3-8. Shielding*

case design.

Figure 3-8. Shielding case design



3.7. Routing and copper pour design

In addition to the requirements for the width of power supply routing and RF routing mentioned above, it is recommended to choose 5 to 6 mil for the width of GPIO lines in the module and the width of GND lines should be at least 8 to 10 mil.

The copper pour of the module PCB should be close to the size of the board frame. More GND vias can be drilled in the blank area in an irregular way before copper pour. One row of GND vias is required to be drilled on the edge of the board. Vias should be placed near each component GND pad. For areas where GND vias can't be placed due to space limitation, no copper is filled to avoid islanding.

4. Package description

GD32VW553 has 2 package types, namely QFN40 and QFN32.

Table 4-1. Description of package types

Product model	Package
GD32VW553Hx	QFN40(5x5, 0.4pitch)
GD32VW553Kx	QFN32(4x4, 0.4pitch)

(dimensions in mm)

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.0	Initial release	Nov.17.2023
1.1	Modify figure2.1&2.6	Mar.1.2024

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