GigaDevice Semiconductor Inc.

Design Guide for Thermal Characteristics of GD32H7xx series

Application Notes
AN166

Revision 1.1

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1. Foreword

This document is specifically formulated for engineering designers developing with the GD32H7xx family of MCUs. It introduces the factors that influence MCU temperature management, heat dissipation methods, and basic thermal management concepts. With the development of semiconductor technology, the integration of circuits within chips keeps increasing, which leads to higher power densities of chips. As the junction temperature (T_J) of a chip rises, the lifespan of the chip decreases, and the failure rate increases. Therefore, the maximum allowable junction temperature for a chip is specified. It must operate below this temperature to maintain its performance and longevity.

This document mainly discusses the thermal characteristics and temperature management solutions for GD32H7xx in high-performance, high-power-consumption scenarios.

2. Choosing Correct Thermal Management Method

2.1. Using System Thermal Characteristic (STC) to Evaluate Thermal Runaway of the System

2.1.1. Power dissipation

There are two types of currents used by MCU:

1. Static Current: Also known as leakage current, it depends on the process, voltage, and junction temperature (T_J), but not on activity.
2. Dynamic Current: It depends on the process, voltage, and activity, but not on junction temperature (T_J) (at least according to recent studies).

This can be expressed in the following equation:

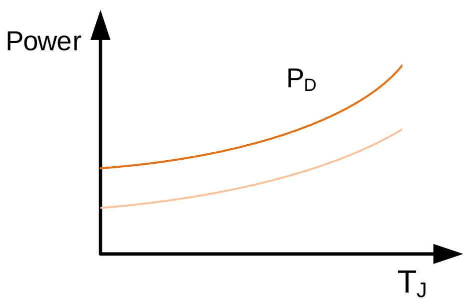
$$I_{Total}(P,V,T_J,Activity)=I_{static}(P,V,T_J)+I_{Dynamic}(P,V,Activity) \quad (2\text{-}1)$$

Static leakage current exponentially increases along with junction temperature, while dynamic current does not.

Power dissipation varies with changes in Process, Voltage, Temperature, and Activity (PVTA) and can be calculated as the product of the voltage generated on MCU and the average current consumed.

In a high-performance, high-power-consumption MCU system, when the program ensures a fixed operation (meaning the dynamic current remains essentially stable), power dissipation is considered to be related only to T_J. Changes in ambient temperature and the system's heat dissipation capability ultimately affect T_J, leading to an exponential change in static current. See *Figure 2-1. TJ-PD curve*.

Figure 2-1. T_J-P_D curve



2.1.2. System thermal resistance (Theta_j_sys)

When the chip operates, the junction temperature rises above the ambient temperature. The temperature difference between them can be calculated as the product of power dissipation and junction-to-ambient thermal resistance:

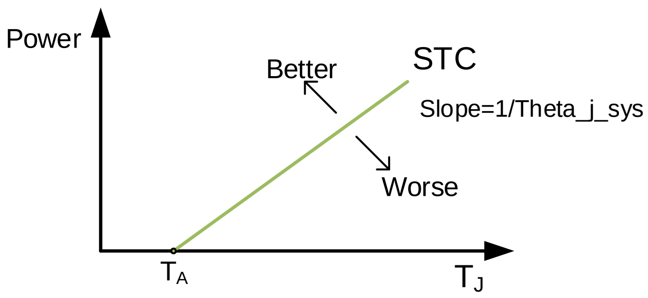
$$T_J=T_A+P_D\times Theta\_j\_sys<T_{J\_max} \quad (2\text{-}2)$$

Where, Theta_j_sys is a simplification of a complex coefficient that is not a characteristic of the chip but that of the system (MCU + other components + circuit board + enclosure + other cooling conditions). The junction temperature must be kept below the maximum target given by the above equation.

Theta_j_sys reflects the system's heat dissipation capability, which can be represented by System Thermal Characteristic (STC):

$$STC=\frac{(T_J-T_A)}{Theta\_j\_sys} \quad (2\text{-}3)$$

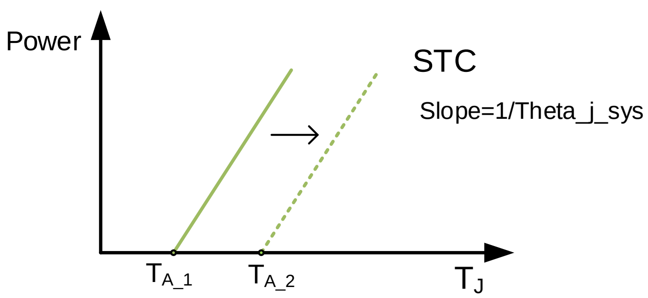
Figure 2-2. System thermal characteristic (STC)



In ***Figure 2-2. System thermal characteristic (STC)*** a greater slope indicates the system has better heat dissipation capability, while a smaller slope indicates the system has poorer heat dissipation capability. The slope represents how good the designed system is in dissipating heat.

Ideally, when the system's cooling method is fixed, the slope of STC remains constant. An increase in ambient temperature causes a rise in the chip's starting temperature to laterally shift the STC curve and obtain STC at different starting temperatures, as shown in ***Figure 2-3. STC linear temperature shift***:

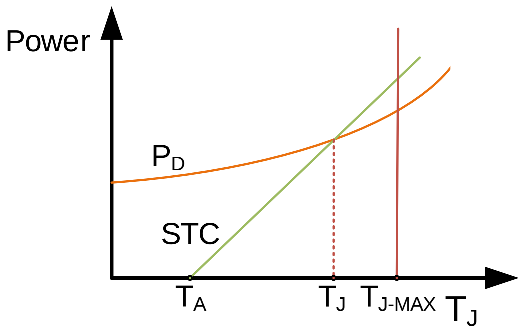
Figure 2-3. STC linear temperature shift



2.1.3. Using STC to evaluate thermal runaway of the system

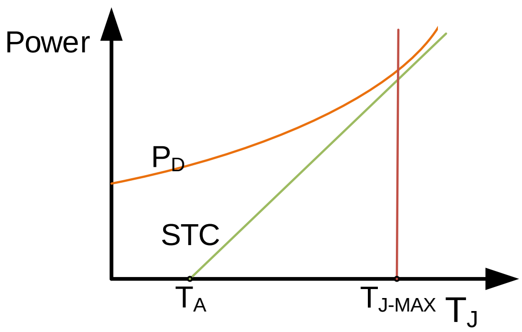
When the system's cooling method is determined and the program is fixed, STC can be used to evaluate thermal runaway of the system. As shown in ***Figure 2-4. Intersection of STC and TJ-PD curve***, if the STC intersects with the T_J-P_D curve and T_J at the intersection is lower than $T_{J\text{-}MAX}$, the system is considered to have no thermal runaway. It represents to which extent the actual power dissipation of the chip matches the system's heat dissipation capacity.

Figure 2-4. Intersection of STC and T_J-P_D curve



However, if the plotted lines do not intersect or if T_J at the intersection is higher than $T_{J\text{-}MAX}$, as shown in ***Figure 2-5. Thermal runaway of system***, the system is considered to have thermal runaway.

Figure 2-5. Thermal runaway of system



Improvements can be made through the following methods to ensure that the intersection lies within the safety margin:

1. Enhance cooling conditions to increase the slope of STC.
2. Reduce or limit the ambient temperature at which the chip operates to move the STC leftward.
3. Modify the program content to reduce power consumption to move the STC downward.

2.1.4. Common methods for improving system cooling

Generally, when a chip operates at a high temperature, its power consumption increases, and its reliability decreases. To ensure better operation and reliability of the chip, it's crucial to select the correct cooling method for the chip.

Selection of appropriate chip package: With the increase in internal chip size, heat can be dissipated over a larger area to enhance the rate of heat dissipation and reduce thermal resistance. Changes in the external package will lead to alterations in the heat dissipation area and path, as well as thermal resistance. Besides the price, layout, and installation, the heat dissipation performance should also be taken into account in selecting a chip package. Especially in scenarios where chips consume a lot of power, the chip package with good heat dissipation can be selected.

Changes in the external environment: Changes in the external environment (such as temperature, wind speed, altitude, etc.) can also lead to changes in the thermal resistance of the system. For example, variations in altitude lead to changes in air pressure and thus in the chip's heat dissipation capability.

Provision of additional devices for cooling: Providing the chip with heat sinks or fans is an effective cooling method.

Effective PCB layout for cooling: Without additional external devices for cooling, most of the heat generated by the chip is dissipated through PCB. Therefore, a good PCB layout is crucial for chip cooling. For chips that require cooling, pouring copper over a large area of PCB below the chip and drilling holes for heat dissipation can effectively dissipate heat. Thickening the poured copper and increasing the number of stacked PCBs (four or more layers recommended) can enhance cooling efficiency. Additionally, separate layout of chips with high heat dissipation can also enhance cooling efficiency.

Sensible power supply design: GD32H7xx is additionally provided with an SMPS module in some packages to improve the power conversion efficiency of the chip and thus significantly reduce temperature rise and power consumption. Temperature rise can also be reduced by directly supplying power to the $V_{0.9V}$ power domain. By designing an appropriate power mode, a balance between temperature rise and performance can be achieved provided that the junction temperature under all working conditions does not exceed 125°C. As listed in ***Table 2-1. GD32H7xx power supply design description:***

Table 2-1. GD32H7xx power supply design description

Mode	Description
1	LDO power supply mode, SMPS power supply mode, featuring low power conversion efficiency, bigger temperature rise.
2	SMPS power supply mode, featuring high power conversion efficiency, minimal temperature rise.
6	Bypass mode, in which power consumption mainly comes from the current externally supplied to V_{CORE}, resulting in a small temperature rise. However, it is essential to ensure the stability and reliability of the external power supply.

Suitable clock frequency: When using the chip, the internal high-precision temperature sensors should be used to detect the chip's temperature. If the temperature is too high, measures such as frequency reduction can be taken.

3. Measurement Example

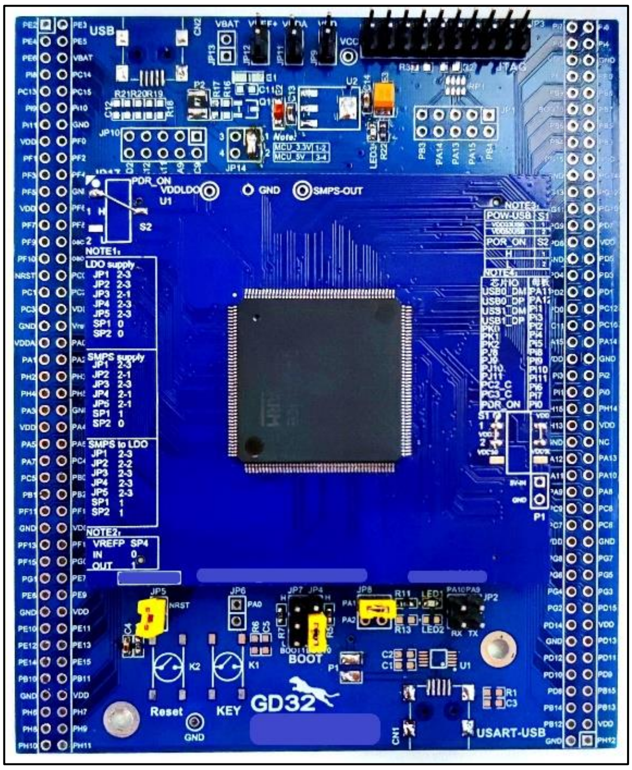
To better demonstrate the relationship between chip temperature rise and power supply method, ambient temperature, and clock frequency, comparative experiments were conducted on chips with different packages in the GD32H7xx series.

3.1. Test Environment

The thermal characteristic experiment in this document was conducted under the following conditions:

1. A motherboard design was used, with the motherboard featuring universal interfaces for necessary communication and power supply. The chip was mounted on a daughterboard, as shown in ***Figure 3-1. Laboratory test hardware***.
2. The reading of the internal high-precision temperature sensor was used as the chip junction temperature, with the condition that it should not exceed the junction temperature for normal and reliable chip operation.
3. Except for the ambient temperature comparison experiment, the ambient temperature for all other experiments was set to the maximum operating temperature specified in the datasheet, 85°C.
4. The data was sourced from extreme samples with maximum values in a batch, for reference purposes only.

Figure 3-1. Laboratory test hardware



3.2. Comparison of Measurement Examples

3.2.1. Power supply method, ambient temperature, package comparison

By changing the power supply method, ambient temperature, and package, the impact on chip temperature rise was observed.

In this case, with a clock frequency of 600 MHz and all peripherals turned on, V_{DD} = V_{DDA} = V_{DDSMPS} = $V_{DD33USB}$ = 3.3V (The input voltage range of GD32H7xx is wide, and the actual power consumption decreases as the power supply voltage decreases. This document takes 3.3V as an example.), and the power supply was set to Mode 2 and Mode 6. When using Mode6, V_{CORE} = 0.9V was injected separately. In this experiment, the reading of the internal high precision sensor was taken as T_J The tested system had no other cooling methods. Experimental data are shown in *Table 3-1. Influence of package, ambient temperature, and power mode on temperature rise*.

Table 3-1. Influence of package, ambient temperature, and power mode on temperature rise

封装	T_A / °C	Mode	T_J / °C	I_{VIN} / mA	I_{CORE} / mA
BGA176	25	6	32	7	190
	85	6	100	7	324
LQFP176	25	2	30	73	-
		6	29	7	187
	85	2	95	140	-
		6	92	7	246
	105	2	120	218	-
LQFP144	25	6	31	7	172
	85	6	92	7	248
LQFP100	25	6	30	7	176
	85	6	94	7	222
BGA100	25	6	31	7	182
	85	6	94	7	245

Notes:

1. I_{VIN} represents the input current to the chip V_{IN} = V_{DD} + V_{DDA} + V_{DDSMPS} + $V_{DD33USB}$. I_{CORE} represents the current injected into the Mode6 V_{CORE} pin. When using Mode 2, the chip's input current is entirely derived from V_{IN}. When using Mode 6, the majority of the chip's input current comes from the injected current into V_{CORE}, with a small portion originating from V_{IN}.

2. In the absence of excellent heat dissipation conditions, if the maximum main frequency is 600MHz, it is recommended to use the power supply mode of each package listed in Table 3-1. For details about the impact of the system heat dissipation design on the temperature rise, see 3.2.3 Summary

3.2.2. Influence of clock frequency on temperature rise

The GD32H7xx series, when operating at high power consumption, may experience a significant increase in junction temperature when using Mode 1 power supply due to the heat generated by the internal LDO at high ambient temperatures. Therefore, it is necessary to lower the clock frequency to ensure the safety of the chip.

This experiment observed the influence of clock frequency on temperature rise by conducting frequency reduction experiments at an ambient temperature of 85°C using Mode1. In this case, all peripherals turned on, V_{DD} = V_{DDA} = V_{DDSMPS} = $V_{DD33USB}$ = 3.3V, and the power supply was set to Mode1. The system had no other cooling methods. The results are shown in ***Table 3-2. Influence of clock frequency on temperature rise***.

Table 3-2. Influence of clock frequency on temperature rise(T_A = 85°C)

Package	Clock frequency / MHz	T_J / °C	I_{VIN} / mA
BGA176	340	117	345
	400	125	412
LQFP176	460	113	266
	520	118	295
LQFP144	340	107	278
	400	109	300
LQFP100	460	109	252
	520	116	280
BGA100	340	109	230
	400	111	254

3.2.3. Influence of system heat dissipation design on temperature rise

Different system PCB designs have a significant impact on temperature rise. The following showcases the evaluation of system heat dissipation performance using BGA176 packaging.

This section uses the same chip (selected from a batch sample with maximum power consumption) mounted on internal test boards A and B, running the same program, and measuring and plotting STC and T_J-P_D curves.

In this case, the clock frequency was set to 600 MHz and all peripherals turned on, V_{DD} = V_{DDA} = V_{DDSMPS} = $V_{DD33USB}$ = 3.3V, and the power supply was set to Mode 1. The system primarily relied on PCB heat dissipation.

The steps are as follows:

1. Determination of STC for two test boards

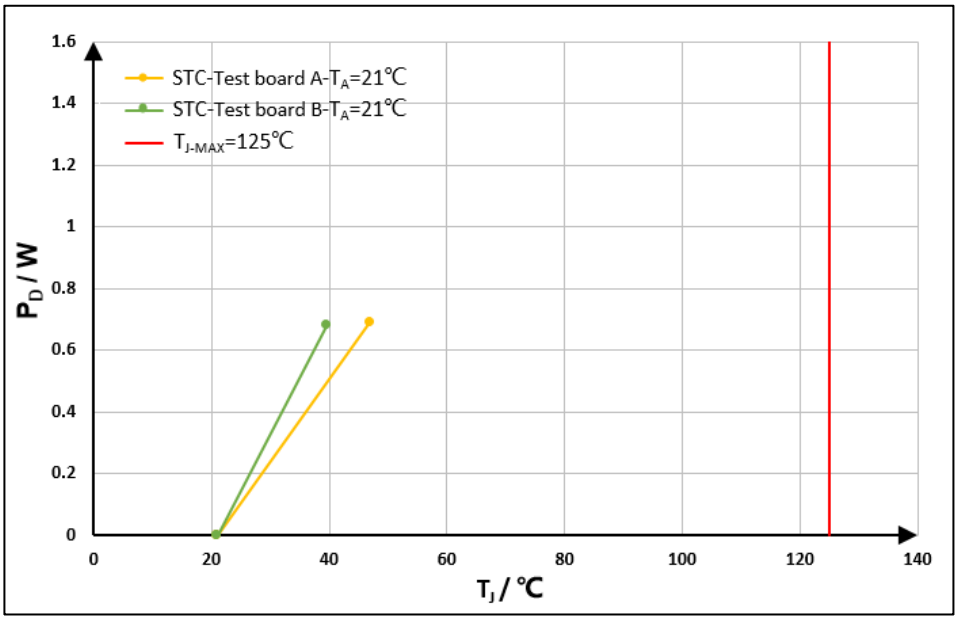
After start-up at room temperature, the input current of the internal test board and T_J were measured to obtain Theta_j_sys, as shown in ***Table 3-3. Calculation of Theta_j_sys for the test boards***:

Table 3-3. Calculation of Theta_j_sys for the test boards

System board	T_A / °C	T_J / °C	I_{VIN} / mA	P_D / W	Theta_j_sys
Test board A	21	47	254	0.838	31.02
Test board B	21	39.6	206	0.68	27.36

Following the table above, the STC can be plotted for two system boards, as shown in ***Figure 3-2. STC straight line plotting***:

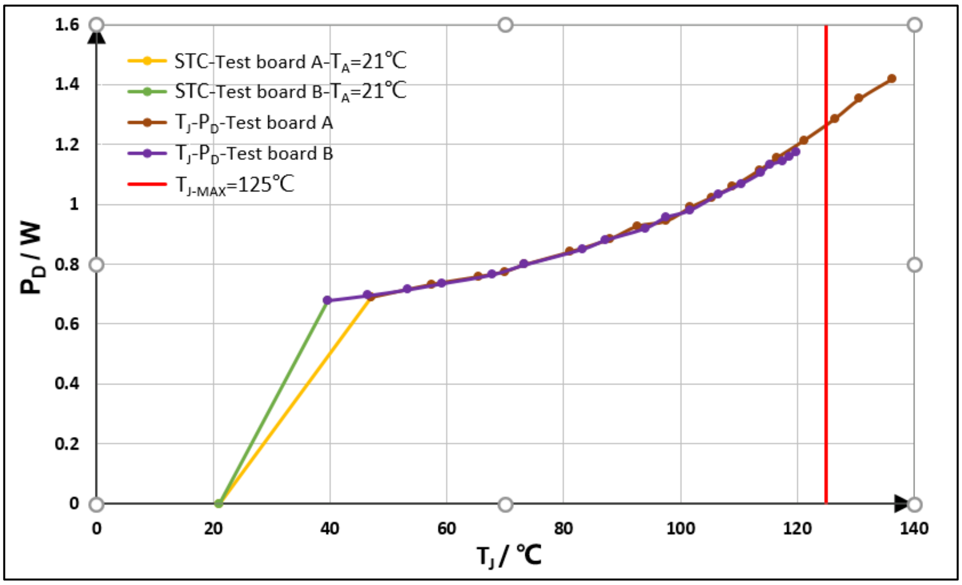
Figure 3-2. STC straight line plotting



2. Plot T_J-P_D curve.

Assuming a fixed testing program, we believe that P_D changes are mainly related to changes in T_J, which can be altered by adjusting the ambient temperature T_A. By placing the test boards in a high temperature environment and monitoring the T_J temperature rise and the subsequent P_D changes after power-on, we can plot the T_J-P_D curve. As shown in ***Figure 3-3. Plot TJ-PD curve***:

Figure 3-3. Plot T_J-P_D curve

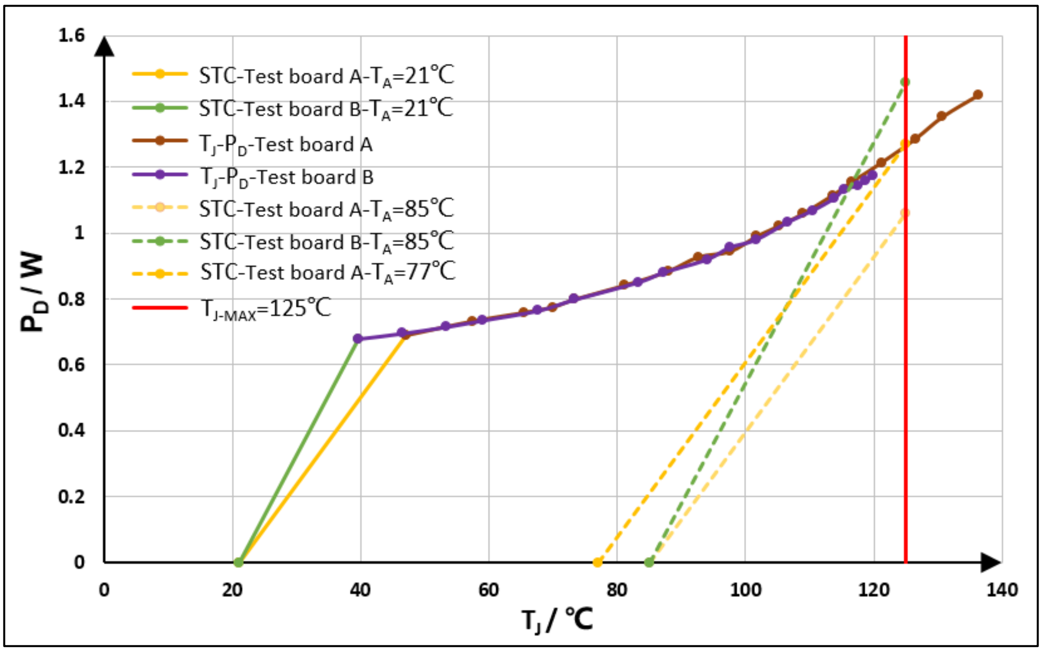


The figure shows that when the same chip is placed on different test boards, the T_J-P_D curves overlap. This indicates that, with a fixed testing program, P_D is primarily influenced by changes in T_J. The design of the system board affects the heat dissipation situation, ultimately impacting changes in T_J.

3. Determine system thermal runaway by shifting STC

To predict high-temperature situations, we can shift both STC straight lines along the coordinate axis. For instance, if T_A = 85°C, as shown in ***Figure 3-4. Shift STC to determine system thermal runaway***.

Figure 3-4. Shift STC to determine system thermal runaway



As shown in the figure above, Test Board A is shifted to the right until T_A = 85°C, showing that STC has no intersection with T_J-P_D curve when T_J is lower than 125°C. This means that the board's heat dissipation performance is inadequate, resulting in the risk of thermal runaway at 85°C. Move the STC to the left until it intersects with the T_J-P_D curve. At this point, it can be observed that the bottom of the straight line, T_A, is approximately 77°C. Therefore, it can be inferred that when the ambient temperature of the test board is around 77°C, T_J equals 125°C, and the ambient temperature for the operation of the test board should not exceed 77°C.

As shown in the figure above, Test Board B is shifted to the right until T_A = 85°C, showing that STC has intersections with T_J-P_D curve when T_J is lower than 125°C. This means that the board's heat dissipation performance is good, without thermal runaway at 85°C.

4. Design and Implementation Suggestions

Here are suggestions for developers to ensure the system reliability when using the GD32H7xx series:

1. In PCB design, ensure the integrity of copper coverage and create heat dissipation vias at the heat generating locations. Place the heat-generating components as far away from the chip as possible.
2. For BGA packages, individually fan out each pin through vias to the GND layer, reducing the trace-to-copper distance to maximize contact area between the central ground pin and the large copper plane, thus ensuring an effective heat dissipation path.
3. Do not remove the dead copper near the chip end on the top/bottom layers. Instead, use multiple vias to connect it to the ground plane, increasing the heat dissipation area.
4. Evaluate the MCU power usage modes comprehensively and Mode 2 and Mode 6 are recommended.
5. Enable internal high-precision temperature sensors to monitor T_J in real-time. If the junction temperature exceeds the maximum specified value of 125°C, proactively lower the frequency to ensure chip safety.
6. If necessary, employ heat sinks, fans, or other means to cool the chip and ensure its reliability.

5. Revision history

Table 5-1. Revision history

Revision No.	Description	Date
1.1	1. Added LQFP176 MODE 2 atmospheric high temperature data. 2. Delete BGA176 MODE 2 high temperature data. 3. Add the precautions in Table 3-1.	Mar. 15, 2024

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