

GigaDevice Semiconductor Inc.

**Migration from GD32L233 series to
GD32L235 series**

**Application Note
AN184**

Table of Contents

| | |
|--|----|
| Table of Contents | 2 |
| List of Figures | 3 |
| List of Tables | 4 |
| 1. Introduction..... | 5 |
| 2. Introduction to hardware differences | 6 |
| 3. Comparison of resource and peripheral..... | 7 |
| 4. Program Migration..... | 10 |
| 5. Peripheral differences | 11 |
| 5.1. Flash memory controller (FMC)..... | 11 |
| 5.2. Power management unit(PMU) | 11 |
| 5.3. Reset and clock unit (RCU)..... | 12 |
| 5.4. Interrupt / event controller (EXTI) | 12 |
| 5.5. DMA request multiplexer (DMAMUX) | 12 |
| 5.6. Debug (DBG) | 13 |
| 5.7. Analog to digital converter (ADC) | 15 |
| 5.8. Timer (TIMERx) | 15 |
| 5.9. Low power timer (LPTIMER) | 16 |
| 5.10. Low-power universal asynchronous receiver/transmitter (LPUART) | 17 |
| 5.11. VREF | 17 |
| 5.12. Segment LCD controller (SLCD) | 17 |
| 5.13. Controller area network (CAN) | 17 |
| 5.14. Universal Serial Bus full-speed device interface (USBD)..... | 18 |
| 6. Revision history..... | 19 |

List of Figures

| | |
|--|----|
| Figure 4-1. The interface for selecting GD32L233xx series and GD32L235xx series for KEIL Project..... | 10 |
| Figure 4-2. The interface for selecting GD32L233xx series and GD32L235xx series for IAR Project..... | 10 |
| Figure 5-1. The comparison of DMAMUX_RM_CHxCFG register between GD32L233xx series and GD32L235xx series..... | 12 |
| Figure 5-2. The comparison of DGB_CTL0 register between GD32L233xx series and GD32L235xx series..... | 13 |
| Figure 5-3. The comparison of DGB_CTL1 register between GD32L233xx series and GD32L235xx series..... | 14 |
| Figure 5-4. The comparison of ADC_CTL1 register between GD32L233xx series and GD32L235xx series..... | 15 |

List of Tables

| | |
|---|----|
| Table 3-1. Overview of Resource Comparison between GD32L235xx Series and GD32L233xx Series | 7 |
| Table 3-2. Overview of GD32L235xx series and GD32L233xx series peripheral address comparison..... | 7 |
| Table 6-1. Revision history..... | 19 |

1. Introduction

The GD32L235xx device is a new 32-bit general-purpose microcontroller base on the ARM® Cortex®-M23 core. It has very high similarity in resources with the GD32L233xx device. This application note aims to help customers quickly port applications from the GD32L233xx series microcontroller to the GD32L235xx series microcontroller.

In order to better use of the information in this application note, customers need to download it from the website www.GD32MCU.com, such as datasheet, user manual, official code and various development tools.

2. Introduction to hardware differences

The package types of the GD32L235xx series include: WLCSP25, QFN32, LQFP32, QFN48, LQFP48, QFN64, LQFP64; The package types of the GD32L233xx series include QFN32, LQFP32, LQFP48, and LQFP64. The pins of the two series of chips with the same package are compatible. There are slight differences in pin definitions between the two series, please refer to the datasheet documentation for details.

3. Comparison of resource and peripheral

There are the following differences in resources between the GD32L235xx series and the GD32L233xx series:

1. The GD32L235xx series has added the number of advanced timers and general timers; The low-power timer of the GD32L235xx series has 16 bits, and the low-power timer of the GD32L233xx series has 32 bits.
2. The GD32L235xx series has added CAN peripheral.
3. The GD32L235xx series has increased the number of LPUART peripherals.

Details can be found in [Table 3-1. Overview of Resource Comparison between GD32L235xx Series and GD32L233xx Series](#), as well as [Table 3-2. Overview of GD32L235xx series and GD32L233xx series peripheral address comparison](#).

Table 3-1. Overview of Resource Comparison between GD32L235xx Series and GD32L233xx Series

| Peripheral | GD32L235xx | GD32L233xx |
|-------------------|-------------|-------------|
| Core | Cortex-M23 | Cortex-M23 |
| Flash | 64K-128K | 64K-256K |
| RAM | 12K-24K | 16K-32K |
| 主频 | 64MHz | 64MHz |
| LPTM | 2(16bit) | 1(32bit) |
| GPTM(16bit) | 5/6 | 3/4 |
| AdvTM(16bit) | 1 | 0 |
| BaseTM(16bit) | 2 | 2 |
| U(S)ART | 3/4 | 3/4 |
| I2C | 3 | 2/3 |
| SPI | 2 | 2 |
| I2S | 1 | 1 |
| USB | 0/1 | 1 |
| CAN | 0/1 | 0 |
| CMP | 2 | 2 |
| ADC | 1(10)/1(16) | 1(10)/1(16) |
| DAC | 1 | 1 |
| SLCD | 0/1 | 0/1 |
| Operating Voltage | 1.62-3.63V | 1.71-3.63V |
| Temperature Range | -40-85°C | -40-85°C |

Table 3-2. Overview of GD32L235xx series and GD32L233xx series peripheral address comparison

| Peripheral | BUS | GD32L235xx | GD32L233xx |
|------------|------|------------|------------|
| GPIOF | AHB2 | 0X48001400 | 0X48001400 |

Migration from GD32L233 series to GD32L235 series

| | | | |
|------------------------------------|------|------------|-------------------------------------|
| GPIOD | | 0X48000C00 | 0X48000C00 |
| GPIOC | | 0X48000800 | 0x48000800 |
| GPIOB | | 0X48000400 | 0X48000400 |
| GPIOA | | 0X48000000 | 0X48000000 |
| TRNG | | 0X50060800 | 0X50060800 |
| CAU | | 0X50060000 | 0X50060000 |
| CRC | | 0X40023000 | 0X40023000 |
| FMC | AHB1 | 0X40022000 | 0X40022000 |
| RCU | | 0X40021000 | 0X40021000 |
| DMAMUX | | 0X40020800 | 0X40020800 |
| DMA | | 0X40020000 | 0X40020000 |
| TIMER40 | | 0X4001D000 | - |
| CMP | | 0X40017C00 | 0X40017C00 |
| DBG | | 0X40015800 | 0X40015800 |
| TIMER8 | | 0X40014C00 | 0X40014C00 |
| TIMER14 | | 0X40014000 | - |
| USART0 | APB2 | 0X40013800 | 0X40013800 |
| SPI0 | | 0X40013000 | 0X40013000 |
| TIMER0 | | 0X40012C00 | - |
| ADC | | 0X40012400 | 0X40012400 |
| EXTI | | 0X40010400 | 0X40010400 |
| SYSCFG+VREF | | 0X40010000 | 0X40010000 |
| CTC | | 0X4000C800 | 0X4000C800 |
| I2C2 | | 0X4000C000 | 0X4000C000 |
| LPTIMER0 | | 0X40009400 | 0X40009400 |
| LPUART0 | | 0X40008000 | 0X40008000(LPUART) |
| LPTIMER1 | | 0X40007C00 | - |
| DAC0 | | 0X40007400 | 0X40007400 |
| PMU | | 0X40007000 | 0X40007000 |
| CAN | | 0X40006400 | - |
| Shared USB/D/CAN RAM(512 bytes) | | 0X40006000 | 0X40006000(USB/D RAM(512 bytes)) |
| USB/D | APB1 | 0X40005C00 | 0X40005C00 |
| I2C1 | | 0X40005800 | 0X40005800 |
| I2C0 | | 0X40005400 | 0X40005400 |
| UART4 | | 0X40005000 | 0X40005000 |
| UART3 | | 0X40004C00 | 0X40004C00 |
| LPUART1 | | 0X40004800 | - |
| USART1 | | 0X40004400 | 0X40004400 |
| SPI1/I2S1 | | 0X40003800 | 0X40003800 |
| FWDGT | | 0X40003000 | 0X40003000 |
| WWDGT | | 0X40002C00 | 0X40002C00 |

Migration from GD32L233 series to GD32L235 series

| | | | |
|---------------|--|------------|------------|
| RTC | | 0X40002800 | 0X40002800 |
| SLCD | | 0X40002400 | 0X40002400 |
| TIMER11 | | 0X40001800 | 0X40001800 |
| TIMER6 | | 0X40001400 | 0X40001400 |
| TIMER5 | | 0X40001000 | 0X40001000 |
| TIMER2 | | 0X40000400 | 0X40000400 |
| TIMER1 | | 0X40000000 | 0X40000000 |
| SRAM | | 0x20000000 | 0x20000000 |
| Option Byte | | 0x1FFFF800 | 0x1FFFF800 |
| Main Flash | | 0x08000000 | 0x08000000 |
| System Memory | | 0x1FFFD000 | 0x1FFFD000 |
| OTP | | 0x1FFF7000 | 0x1FFF7000 |

4. Program Migration

The GD32L233xx series and GD32L235xx series both belong to the GD32L23x series, and the new version of the firmware library GD32L23x_ Firmware_Library (version 2.0.0 and above) is already compatible with two series of products, GD32L233xx and GD32L235xx. When using the new version of the firmware library, simply select the corresponding series, as shown in [Figure 4-1. The interface for selecting GD32L233xx series and GD32L235xx series for KEIL Project](#) and [Figure 4-2. The interface for selecting GD32L233xx series and GD32L235xx series for IAR Project](#) is shown.

Figure 4-1. The interface for selecting GD32L233xx series and GD32L235xx series for KEIL Project

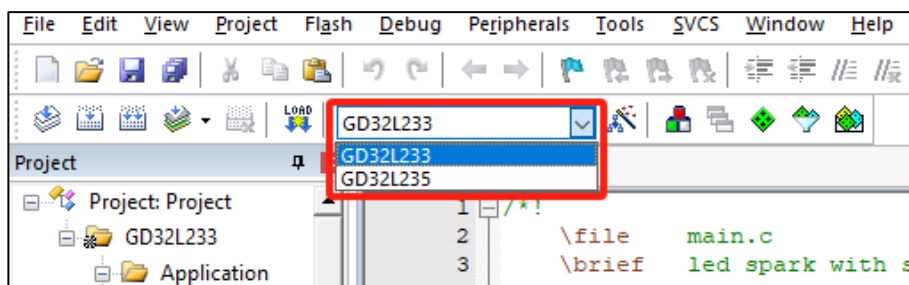
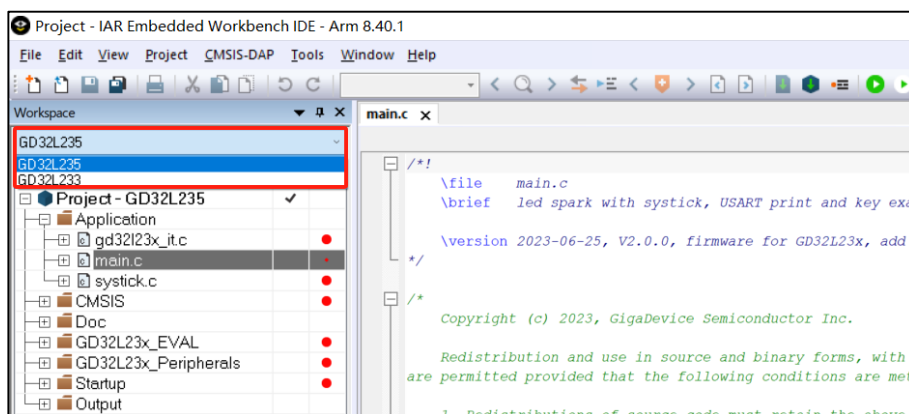


Figure 4-2. The interface for selecting GD32L233xx series and GD32L235xx series for IAR Project



If GD32L235xx is running an older version of the firmware library, please refer to Chapter 5 for any issues that need to be noted.

5. Peripheral differences

GD32L235xx is compatible with GD32L233xx in some peripherals, but as a more advanced MCU, GD32L235xx has added some features on many peripherals compared to GD32L233xx. Users can port their code based on the differences in peripherals listed below.

5.1. Flash memory controller (FMC)

When using FMC code, it is important to pay attention to the following points:

1. For GD32L233xx, the flash page size is 4/2/1KB, depending on different flash density. For GD32L235xx, the flash page size is 1KB.
2. For GD32L233xx, word programming, page erase and mass erase operation supported. For GD32L235xx, double-word programming, page erase and mass erase operations supported.
3. Fast program supported (only available in GD32L233).
4. ECC check supported (only available in GD32L235)
5. For GD32L233xx product, flash can work at LDO 1.1V and 0.9V; For GD32L235xx, flash only works at LDO 1.1V.
6. The option byte USER section of GD32L235xx product has an enable bit for SRAM parity check, while GD32L233xx product does not.

5.2. Power management unit (PMU)

For GD32L233xx devices:

1. Internal Voltage regulator (LDO) supplies around 1.1V or 0.9V voltage source for 1.1V domain.
2. Ten power saving modes: Run, Run1, Run2, Sleep, Sleep1, Sleep2, Deep-sleep, Deep-sleep 1, Deep-sleep 2 and Standby modes.
3. CAU can be power off alone.

For GD32L235xx devices:

1. Internal Voltage regulator (LDO) supplies around 1.1V source for 1.1V domain.
2. Six power saving modes: Run, Sleep, Deep-sleep, Deep-sleep 1, Deep-sleep 2 and Standby modes.
3. Internal Voltage regulator (LDO) supplies around 0.9V voltage source for 1.1V domain when in Deep-sleep 1 or Deep-sleep 2 mode.

4. EFLASH can be power-off alone when in run or Deep-sleep mode.

5.3. Reset and clock unit (RCU)

1. For GD32L233xx devices, the LPUART is clocked by IRC16MDIV clock or LXTAL clock or system clock or APB1 clock, which selected by LPUARTSEL bits in configuration register 2 (RCU_CFG2). For GD32L235xx devices, the LPUARTx(x = 0, 1) is clocked by IRC16MDIV clock or LXTAL clock or system clock or APB1 clock, which selected by LPUARTxSEL(x = 0, 1) bits in configuration register 2 (RCU_CFG2).
2. For GD32L233xx devices, the LPTIMER is clocked by IRC16MDIV clock or LXTAL clock or system clock or APB1 clock, which selected by LPTIMERSEL bits in configuration register 2(RCU_CFG2). For GD32L235xx devices, the LPTIMERx(x = 0, 1) is clocked by IRC16MDIV clock or LXTAL clock or system clock or APB1 clock, which selected by LPTIMERxSEL(x = 0,1) bits in configuration register 2 (RCU_CFG2).
3. The GD32L23x's system clock (CK_SYS) which can source from the IRC16M, IRC48M, HXTAL, IRC32K (Only for GD32L235 devices) or PLL. The system clock source of GD32L233xx product does not include IRC32K.

5.4. Interrupt / event controller (EXTI)

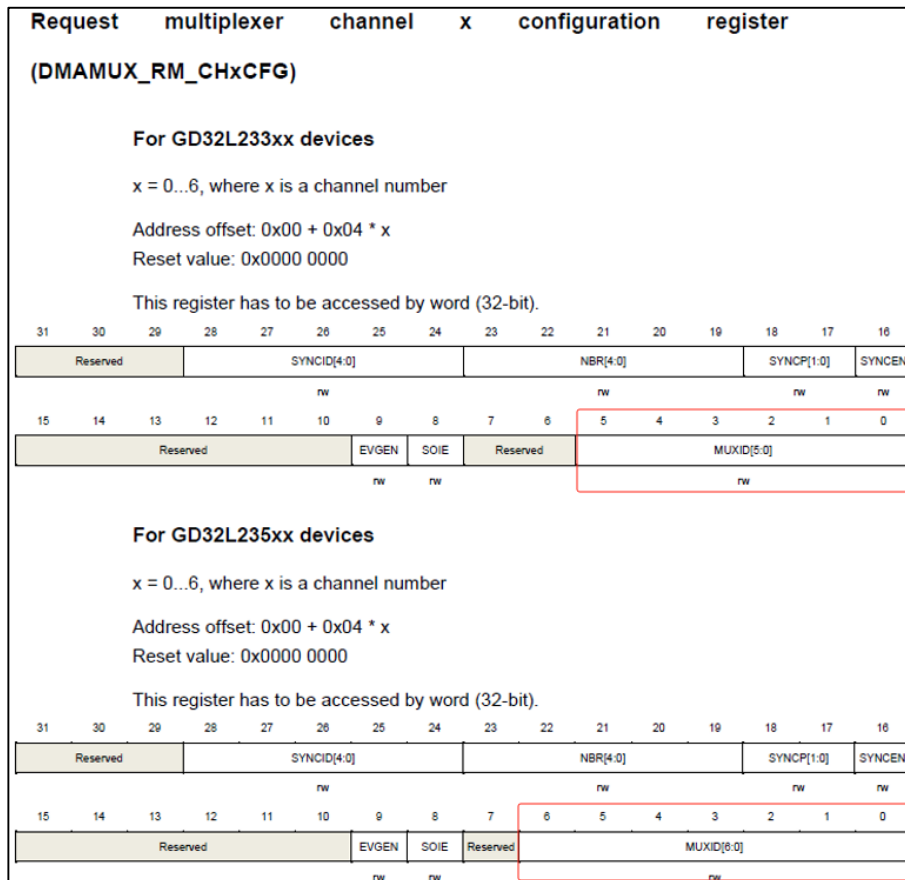
1. Up to 69 maskable peripheral interrupts (for GD32L233xx devices) or 72 maskable peripheral interrupts (for GD32L235xx devices).
2. Up to 30 independent edge detectors (for GD32L233xx devices) or 32 independent edge detectors (for GD32L235xx devices) in EXTI.

5.5. DMA request multiplexer (DMAMUX)

A DMA request input for the DMAMUX request multiplexer channel x is configured by the MUXID[5:0] (for GD32L233xx devices)/ MUXID[6:0](for GD32L235xx devices) bits in the DMAMUX_RM_CHxCFG register. See [Figure 5-1. The comparison of DMAMUX_RM_CHxCFG register between GD32L233xx series and GD32L235xx series](#), specific usage can be found in the Request multiplexer input mapping in the GD32L23x user manual.

Figure 5-1. The comparison of DMAMUX_RM_CHxCFG register between GD32L233xx

series and GD32L235xx series



5.6. Debug (DBG)

The DBG hold unit helps debugger to debug power saving mode, TIMER, LPTIMER, I2C, CAN, RTC, WWDGT, and FWDGT. When the core is halted and the corresponding bit in DBG control register 0 or DBG control register 1 (DBG_CTL0 or DBG_CTL1) is set, it provides a clock in power saving mode or holds the state for TIMER, LPTIMER, I2C, CAN, RTC, WWDGT and FWDGT. Due to differences in peripherals between L233xx and L235xx series, the difference of DGB_ CTL0 and DBG_ CTL1 register is shown in [Figure 5-2. The comparison of DGB_ CTL0 register between GD32L233xx series and GD32L235xx series](#) and [Figure 5-3. The comparison of DGB_ CTL1 register between GD32L233xx series and GD32L235xx series](#). Attention should be paid when using this feature.

Figure 5-2. The comparison of DGB_ CTL0 register between GD32L233xx series and

GD32L235xx series

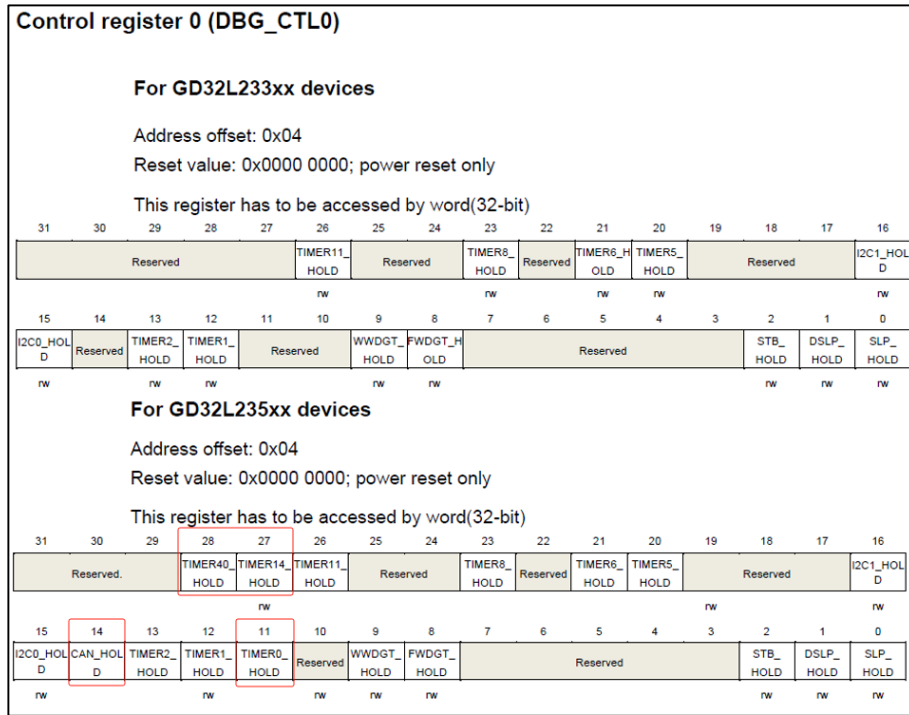
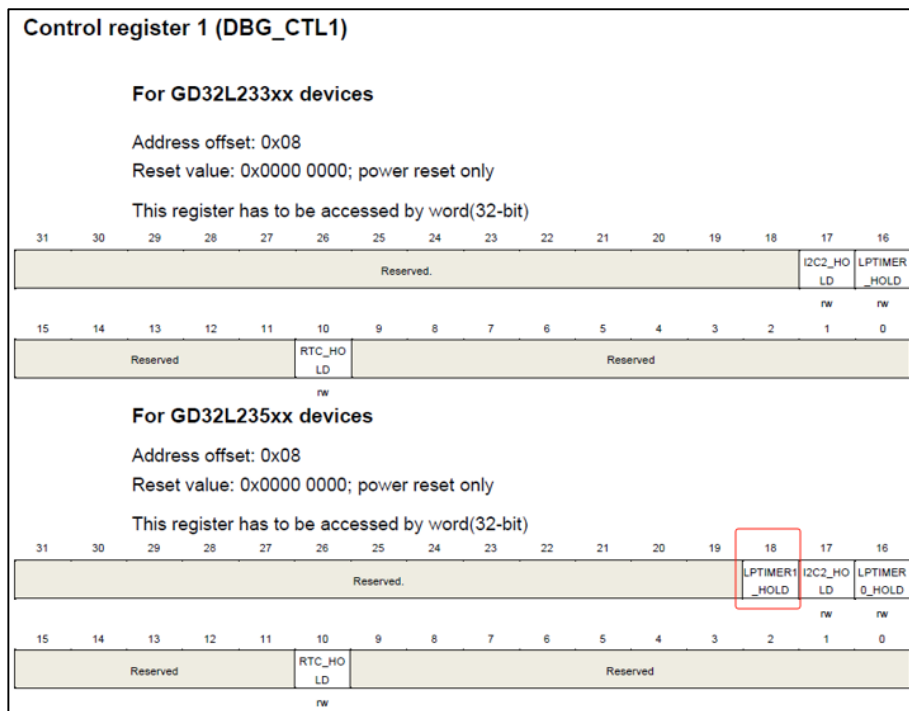


Figure 5-3. The comparison of DGB_CTL1 register between GD32L233xx series and GD32L235xx series



5.7. Analog to digital converter (ADC)

1. In GD32L23xx series, only available for GD32L235xx devices. By writing into bits DIFCTL[14:0] in the ADC_DIFCTL register, the user can configure channels as differential input or single-ended input. The GD32L233xx devices only support single-ended input mode.
2. The GD32L235xx devices support the configuration of calibration times, while the GD32L233xx devices do not support this function, as shown in [Figure 5-4. The comparison of ADC_CTL1 register between GD32L233xx series and GD32L235xx series.](#)

Figure 5-4. The comparison of ADC_CTL1 register between GD32L233xx series and GD32L235xx series

| Control register 1 (ADC_CTL1) | | | | | | | | | | | | | | | |
|---|----|----|----|---------|----------|---------|-------|----------|-------------|-------|-------------|-----|-----|----------|----|
| For GD32L233xx devices | | | | | | | | | | | | | | | |
| Address offset: 0x08 | | | | | | | | | | | | | | | |
| Reset value: 0x0000 0000 | | | | | | | | | | | | | | | |
| This register has to be accessed by word(32-bit). | | | | | | | | | | | | | | | |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | VSLCDEN | VBATEN | INREFEN | TSVEN | SWRCST | Reserved | ETERC | ETSRC [2:0] | | | Reserved | |
| | | | | rw | rw | rw | rw | rw | | rw | rw | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | DAL | Reserved | | DMA | Reserved | | | RSTCLB | CLB | CTN | ADCON | |
| | | | | rw | | | rw | | | | rw | rw | rw | rw | |
| For GD32L235xx devices | | | | | | | | | | | | | | | |
| Address offset: 0x08 | | | | | | | | | | | | | | | |
| Reset value: 0x0000 0000 | | | | | | | | | | | | | | | |
| This register has to be accessed by word(32-bit). | | | | | | | | | | | | | | | |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Reserved | | | | VSLCDEN | VBATEN | INREFEN | TSVEN | SWRCST | Reserved | ETERC | ETSRC [2:0] | | | Reserved | |
| | | | | rw | rw | rw | rw | rw | | rw | rw | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | DAL | Reserved | | DMA | Reserved | CALNUM[2:0] | | RSTCLB | CLB | CTN | ADCON | |
| | | | | rw | | | rw | rw | | rw | rw | rw | rw | | |

5.8. Timer (TIMERx)

For GD32L235xx devices: Advanced TIMER0、General level0 TIMER1/2、General level1 TIMER8/11、General level3 TIMER14/40、Basic TIMER5/6.

For GD32L233xx devices: General level0 TIMER1/2、General level1 TIMER8/11、Basic TIMER5/6.

The two series have the same configuration for handling basic timers 5/6, but have the following differences.

1. Clock source configuration for GD32L23x:

Migration from GD32L233 series to GD32L235 series

- For GD32L235xx devices: The TIMER has the capability of being clocked by either the CK_TIMER or an alternate clock source controlled by SMC (TIMERx_SMCFG bit[2:0]).
 - For GD32L233xx devices: The TIMER has the capability of being clocked by either the CK_TIMER or an alternate clock source controlled by TSCFGy[3:0] in SYSCFG_TIMERxCFG (y=0,1...7) (x=0,1,2,8,11,14,40).
2. Mode selection of Quadrature decoder
 - For GD32L233, the mode is selected by setting the SMC[2:0] to 0x01, 0x02 or 0x03.
 - For GD32L235, the mode is selected by setting TSCFGy[3:0] != 4'b0000 (y=0,1,2).
 3. Master-slave management

The TIMERx can be synchronized with a trigger in several modes including the restart mode, the pause mode and the event mode.

- For GD32L233, these modes are selected by the SMC [2:0] in the TIMERx_SMCFG register. The trigger input of these modes can be selected by the TRGS [2:0] in the TIMERx_SMCFG register.
 - For GD32L235, these modes are selected by the TSCFGy[3:0] != 4b'0000 in SYSCFG_TIMER1CFG or SYSCFG_TIMER2CFG (y=3,4,5), The trigger input of these modes can be selected by the TSCFGy[3:0] in SYSCFG_TIMER1CFG or SYSCFG_TIMER2CFG, different TSCFGy[3:0] is correspond to different trigger input.
4. Timers interconnection

The timers can be internally connected together for timer chaining or synchronization. This can be implemented by configuring one timer to operate in the master mode while configuring another timer to be in the slave mode.

TIMER2 as prescaler for TIMER1 ,Select the TIMER1 input trigger source from TIMER2 and configure TIMER1 in external clock mode 1.

- For GD32L233, setting TRGS=000 in the TIMER1_SMCFG register and setting SMC=111 in TIMER1_SMCFG register.
- For GD32L235, setting TSCFG6[3:0] = 0001 in the _SYSCFG_TIMERxCFG register.

Note: As can be seen from the above, the GD32L235xx series requires the SYSCFG clock to be turned on before configuring TIMER.

5.9. Low power timer (LPTIMER)

The GD32L233xx has one 32-bit LPTIMER, while the GD32L235xx has two 16 bit LPTIMER

(LPTIMER0, LPTIMER1).

5.10. Low-power universal asynchronous receiver/transmitter (LPUART)

The GD32L233xx has one LPUART, while the GD32L235xx has two LPUARTs (LPUART0, LPUART1).

5.11. VREF

The GD32L235xx can provides 2.5V/2.048V reference voltage, while GD32L233XX can only provides 2.5V reference voltage.

5.12. Segment LCD controller (SLCD)

1. For GD32L233 series, the SLCD module integrates an optional voltage output driver, which can enter the enhanced mode by enabling the VODEN bit of the SLCD_CTL register. GD32L235 series does not support enhance mode.
2. GD32L235xx supports weak driving resistance selection, but GD32L233xx does not.
3. For GD32L233 series, when using the internal voltage, the VSLCD value can be selected from VSLCD0 to VSLCD7 by the CONR[2:0] bits in the SLCD_CFG register (Refer to the product datasheet for the VSLCDx values). The application can adjust the contrast according to the change of VSLCD value. For GD32L235 series, when using the internal voltage, when using the internal voltage, the VDD voltage as internal voltage source.
4. VSLCD voltage source configuration, Internal voltage source:
 - For GD32L233 series, when the SLCD selects the internal voltage source, the VSRC should be configured 1' b0 and the PD6 pin needs to be configured in analog mode. A external capacitor should be connected to GND. Please refer to Datasheet for the capacitance value.
 - For GD32L235 series, when the SLCD selects the internal voltage source, the VDD voltage as internal voltage.

5.13. Controller area network (CAN)

The GD32L235xx series has added CAN peripheral, while the GD32L233xx series do not.

5.14. Universal Serial Bus full-speed device interface (USBD)

1. For GD32L233xx device, the frequency of the APB1 bus clock must be not less than 24MHz. For GD32L235xx device, the frequency of the APB1 bus clock must be not less than 12MHz.
2. For GD32L235xx device, the USBD and CAN share the dedicated 512-byte SRAM memory.

6. Revision history

Table 6-1. Revision history

| Revision No. | Description | Date |
|--------------|-----------------|-------------|
| 1.0 | Initial Release | Jan.10 2024 |

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